COMX-P40x0 ENP2

Installation and Use

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About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices.

- *Safety Notes* summarizes the safety instructions in the manual.
- *Sicherheitshinweise*,provides the German translation of the safety notes section.
- *Introduction* provides an overview of the module's features.
- *Hardware Preparation and Installation* provides instructions for installing and removing the module.
- *Controls, LEDs, and Connectors* provides pin assignments for the various connectors on the module.
- *Functional Description* describes the functions of the various components on the module.
- *Clock Structure* describes the clock distribution and the setup utility used to configure the module.
- *Power Domains* describes the power supply system for the module.
- *BSP* describes how to build the Basic Support Package (BSP) and deploy the built images on the module.
- *Related Documentation* provides a list of related product documentation, manufacturer's documents, and industry standard specifications.

Abbreviations

This document uses the following abbreviations:

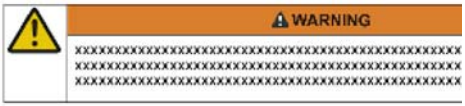
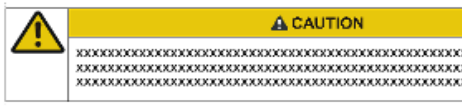
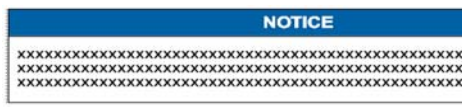
TERM	MEANING
BSP	Board Support Package
GPIO	General Purpose Input Output
I2C	Inter Integrated Circuit
MDIO	Management Data Input/Output
MMC	Module Management Controller
PCI	Peripheral Component Interface

TERM	MEANING
PCI E	Peripheral Component Interface Express
PHY	Ethernet controller physical layer device
RCW	Reset Control Word
RTC	Real Time Clock
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SATA	Serial AT Attachment: serial-interface standard for hard disks
SBC	Single Board Computer
SD	Secure Digital
SDHC	Secure Digital High Capacity
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watch Dog Timer.

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu

Notation	Description
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800R95A	August, 2013	Initial version
6806800R95B	August, 2014	Re-branded to Artesyn template
6806800R95C	January 2015	Removed the references to SCP-P4040-4G-ENP2.

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn Embedded Technologies intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Artesyn or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Artesyn representative for service and repair to make sure that all safety features are maintained.

EMC

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. Changes or modifications not expressly approved by Artesyn Embedded Technologies could void the user's authority to operate the equipment. Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a compliant system will maintain the required performance. Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained.

Operation

Product Damage
High humidity and condensation on the board surface causes short circuits.
Do not operate the board outside the specified environmental limits.
Make sure the board is completely dry and there is no moisture on any surface before applying power.

Damage of Circuits
Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Board Malfunction
Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their setting is changed.
Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

Installation

Data Loss
Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

Make sure all software is completely shut down before removing power from the board or removing the board from the chassis.

Product Damage
Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Product Damage
Inserting or removing modules with power applied may result in damage to module components.
Before installing or removing additional devices or modules, read the documentation that came with the product.

Cabling and Connectors

Product Damage
RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

Battery

Board/System Damage
Incorrect exchange of lithium batteries can result in a hazardous explosion.
When exchanging the onboard lithium battery, make sure that the new and the old battery are exactly the same battery models.
If the respective battery model is not available, contact your local Artesyn sales representative for the availability of alternative, officially approved battery models.

Data Loss
Exchanging the battery can result in loss of time settings. Backup power prevents the loss of data during exchange.
Quickly replacing the battery may save time settings.

Data Loss
If the battery has low or insufficient power the RTC is initialized.
Exchange the battery before seven years of actual battery use have elapsed.

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

Environment

Environmental Damage
Improperly disposing of used products may harm the environment.
Always dispose of used products according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

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Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Artesyn. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

EMV

Das Produkt wurde in einem Artesyn Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produktes in Gewerbe- sowie Industriegebieten gewährleisten.

Das Produkt arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Wird das Produkt in einem Wohngebiet betrieben, so kann dies mit grosser Wahrscheinlichkeit zu starken Störungen führen, welche dann auf Kosten des Produktanwenders beseitigt werden müssen. Änderungen oder Modifikationen am Produkt, welche ohne ausdrückliche Genehmigung von Artesyn durchgeführt werden, können dazu führen, dass der Anwender die Genehmigung zum Betrieb des Produktes verliert. Boardprodukte werden in einem repräsentativen System getestet, um zu zeigen, dass das Board den oben aufgeführten EMV-Richtlinien entspricht. Eine ordnungsgemässe Installation in einem System, welches die EMV-Richtlinien erfüllt, stellt sicher, dass das Produkt gemäss den EMV-Richtlinien betrieben wird. Verwenden Sie nur abgeschirmte Kabel zum Anschluss von Zusatzmodulen. So ist sichergestellt, dass sich die Aussendung von Hochfrequenzstrahlung im Rahmen der erlaubten Grenzwerte bewegt.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Betrieb

1 Beschädigung des Produktes
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Produktes können zu Kurzschlüssen führen.
Betreiben Sie das Produkt nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Produkt kein Kondensat befindet.

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Fehlfunktion des Produktes
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ggf. ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Produkt installieren.

Installation

Datenverlust
Das Herunterfahren oder die Deinstallation eines Boards bevor das Betriebssystem oder andere auf dem Board laufende Software ordnungsmemäss beendet wurde, kann zu partiellem Datenverlust sowie zu Schäden am Filesystem führen.
Stellen Sie sicher, dass sämtliche Software auf dem Board ordnungsgemäss beendet wurde, bevor Sie das Board herunterfahren oder das Board aus dem Chassis entfernen.

Beschädigung des Produktes
Fehlerhafte Installation des Produktes kann zu einer Beschädigung des Produktes führen.
Verwenden Sie die Handles, um das Produkt zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass das Face Plate oder die Platine deformiert oder zerstört wird.

Beschädigung des Produktes und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Produktes und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Kabel und Stecker

Beschädigung des Produktes
Bei den RJ-45-Steckern, die sich an dem Produkt befinden, handelt es sich entweder um Twisted-Pair-Ethernet (TPE) oder um E1/T1/J1-Stecker. Beachten Sie, dass ein versehentliches Anschließen einer E1/T1/J1-Leitung an einen TPE-Stecker das Produkt zerstören kann.

- Kennzeichnen Sie deshalb TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.
- Stellen Sie sicher, dass die Länge eines mit Ihrem Produkt verbundenen TPE-Kabels 100 m nicht überschreitet.
- Das Produkt darf über die TPE-Stecker nur mit einem Sicherheits-Kleinspannungs-Stromkreis (SELV) verbunden werden.

Bei Fragen wenden Sie sich an Ihren Systemverwalter.

Batterie

Beschädigung des Blades
Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.

Datenverlust
Wenn Sie die Batterie austauschen, können die Zeiteinstellungen verloren gehen. Eine Backupversorgung verhindert den Datenverlust während des Austauschs.
Wenn Sie die Batterie schnell austauschen, bleiben die Zeiteinstellungen möglicherweise erhalten.

Datenverlust
Wenn die Batterie wenig oder unzureichend mit Spannung versorgt wird, wird der RTC initialisiert.
Tauschen Sie die Batterie aus, bevor sieben Jahre tatsächlicher Nutzung vergangen sind.

Schäden an der Platine oder dem Batteriehalter
Wenn Sie die Batterie mit einem Schraubendreher entfernen, können die Platine oder der Batteriehalter beschädigt werden.
Um Schäden zu vermeiden, sollten Sie keinen Schraubendreher zum Ausbau der Batterie verwenden.

Umweltschutz

Falsche Entsorgung der Produkte schadet der Umwelt.
Entsorgen Sie alte Produkte gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

1.1 Overview

The COMX-P40x0-ENP2 is a COM Express module based on the Freescale QorIQ™ processors on convenient pluggable mezzanine modules that is suitable for use in extended temperature, rugged environments. The COMX-P40x0 module provides a high-performance, feature-rich solution for current and future generations of embedded applications.

Following are the features of the COMX-P40x0 ENP2 module:

- Supports Freescale QorIQ P4040 or P4080 processors
- Form Factor: Basic (95 mm x 125 mm)
- Memory: 2 GB or 4 GB soldered-down DDR3-1333 with ECC
  - Designed to support up to 8 GB of DDR3
- Sixteen configurable SerDes lanes routed to COM Express connectors. Available interfaces include: PCIE, XAUI, SRIO, SGMII
- On-board Storage:
  - 16bit NOR FLASH from local bus (standard product default)
  - NAND FLASH from local bus
  - I2C EEPROM

    Note: Selectable via carrier
- Software: Demo, runtime Linux Operating System and filesystem(s), pre-installed in NOR/NAND Flash.

I/O Connectors:

- Four UART ports
- One Gigabit Ethernet interface (10/100/1000Base-T)
- Four USB ports
- IEEE 1588 control
- Three I^2C bus
- Eight GPIO ports
- SPI bus with four chip select signals

- Secure Digital Host Controller interface to the COM Express connector for MultiMediaCard (MMC) and Secure Digital card (SD) support.
- Tamper detect pin to the COM connectors
- On-board Real Time Clock (RTC) and Watch Dog Timer (WDT) device
- Provide both remote and local thermal sensor
- JTAG connector on module
- Aurora testing points on module
- 12 V power supplied to module through COM connectors
- Two MDIO
- Five IRQ interrupts
- One SDIO
- 5 V standby power from COM connector not required/used by module

NOTICE

Due to P4080 errata GEN-A009, Aurora ports are disabled by default in RCW and must be re-enabled for debug. For assistance, contact Artesyn representative.

1.2 Standard Compliances

The product is designed to meet the following standards.

Table 1-1 Standard Compliances

Standard	Description
UL60950-1 EN 60950-1 IEC 60950-1 CAN/CSA C22.2 No 60950-1	Safety Requirements
UL/CSA 60950-1 EN 60950-1 IEC 60950-1 CB Scheme	Legal safety requirements

Table 1-1 Standard Compliances (continued)

Standard	Description
FCC 47 CFR Part 15 Subpart B (US), Class A EN55022 Class A (EU) AS/NZS CISPR 22 Class A (Australia/New Zealand) VCCI Class A (Japan)	EMC requirements (legal) on system level (predefined Artesyn system)
CISPR 22 CISPR 24 EN55022 EN 55024	EMC Requirements on system level
ETSI EN 300 019 Series	Environmental Requirement
Directive 2011/65/EU	Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (ROHS)

The following figure contains the declaration of conformity for COMX-P40x0.

Figure 1-1 Declaration of Conformity

EC Declaration of Conformity

According to EN 17050-1:2004

Manufacturer's Name:	Artesyn Embedded Technologies Embedded Computing
Manufacturer's Address:	Zhongshan General Carton Box Factory Co. Ltd. No 62, Qi Guan Road West, Shiqi District, 528400 Zhongshan City Guangdong, PRC

Declares that the following product, in accordance with the requirements of 2004/108/EC, 2006/95/EC, 2011/65/EU and their amending directives,

Product:	COMX-P40x0-ENP2—Express Form Factor Processor Pluggable Mezzanine Module For Extended Temperature and rugged Environments
Model Name/Number:	COMX-P4040-4G-ENP2, COMX-P4080, COMX-P4080-2G-E-ENP2, COMX-P4080-2G-ENP2, COMX-P4080-4G-E-ENP2, COMX-P080-4G-ENP2

has been designed and manufactured to the following specifications:

EN55022: 2010 Class B

EN55024: 2010

IEC 60950-1: 2005 (2nd Edition) + A1: 2009

2011/65/EU RoHS Directive

As manufacturer we hereby declare that the product named above has been designed to comply with the relevant sections of the above referenced specifications. This product complies with the essential health and safety requirements of the above specified directives. We have an internal production control system that ensures compliance between the manufactured products and the technical documentation.

Tom Tuttle, Manager, Product Testing Services

07/30/2014
Date (MM/DD/YYYY)

CE

ARTESYN EMBEDDED TECHNOLOGIES

1.3 Mechanical Data

This section provides mechanical details of COMX-P4080-ENP2 and COMX-P4040-ENP2 modules.

Figure 1-2 COMX-P40x0-ENP2 Top View

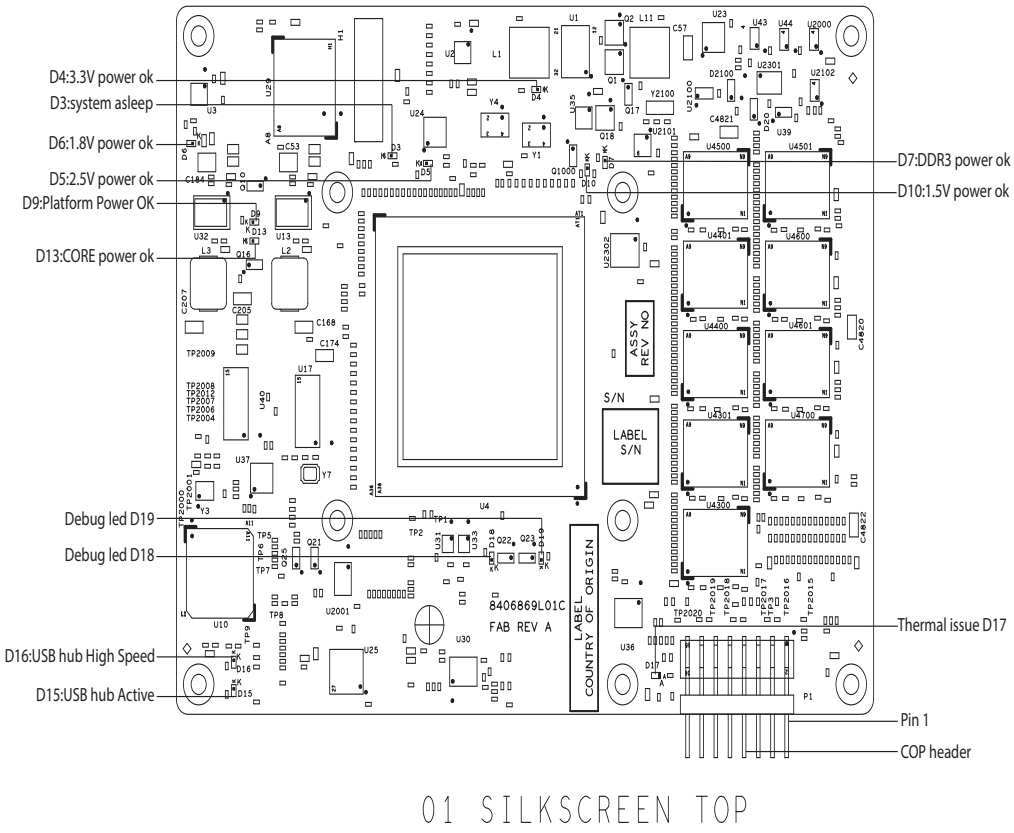
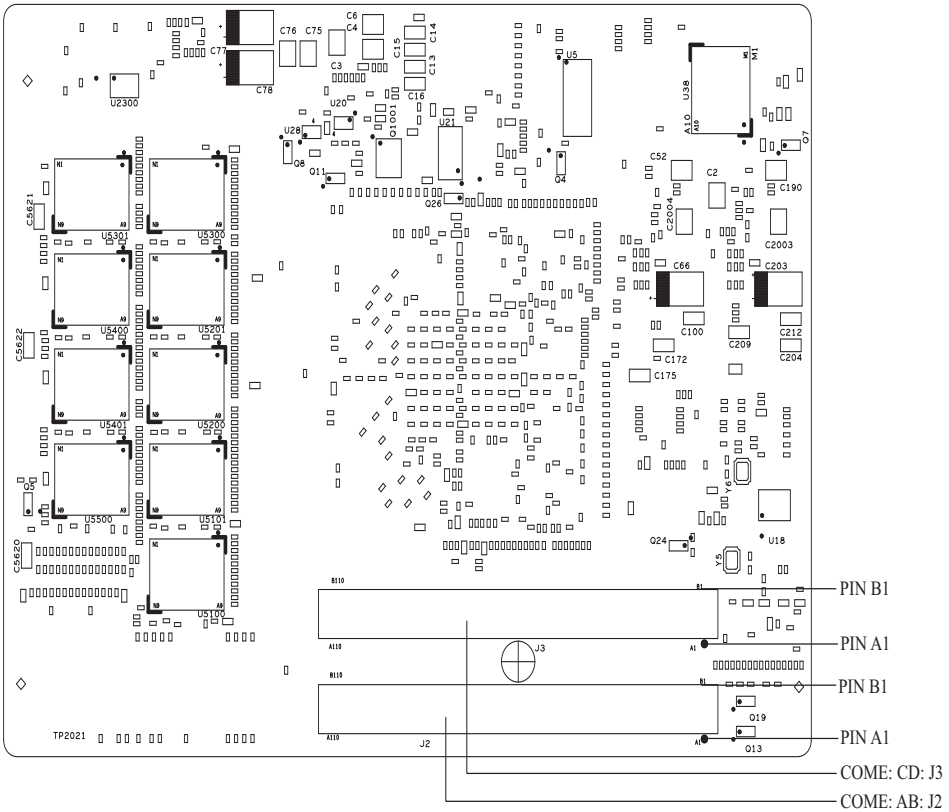


Figure 1-3 COMX-P40x0-ENP2 Bottom View



1.3.1 COMX-P4080 ENP2

The following figure illustrates the top and side views of the COMX-P4080 ENP2 module.

Figure 1-4 COMX-P4080 ENP2 Mechanical Dimensions (Top and side views)

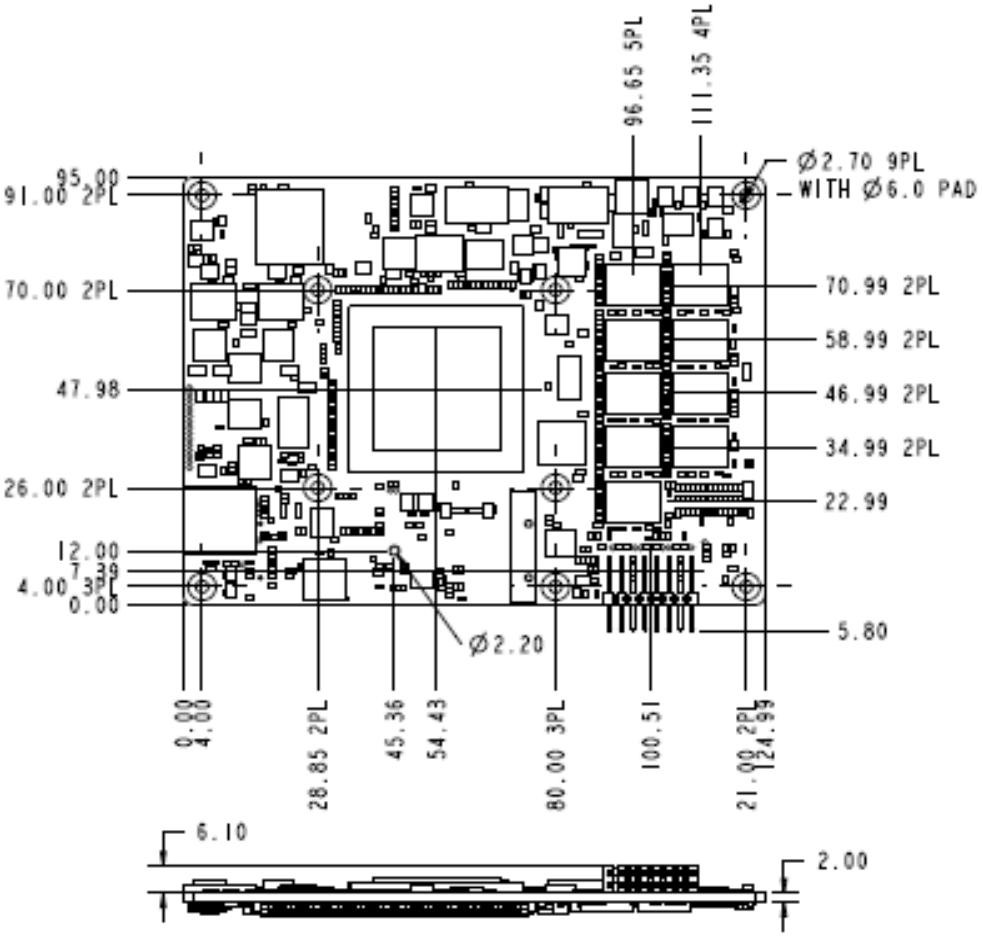


Table 1-2 COMX-P4080 ENP2 Module Dimensions

Characteristic	Value
Length	125 mm
Width	95 mm
Thickness	2 mm
Mounting height top side (component side 1)	6.1 mm

1.3.2 COMX-P4040 ENP2

The following figure illustrates the top and side views of the COMX-P4040 ENP2 module.

Figure 1-5 COMX-P4040 ENP2 Mechanical Dimensions (Top and side views)

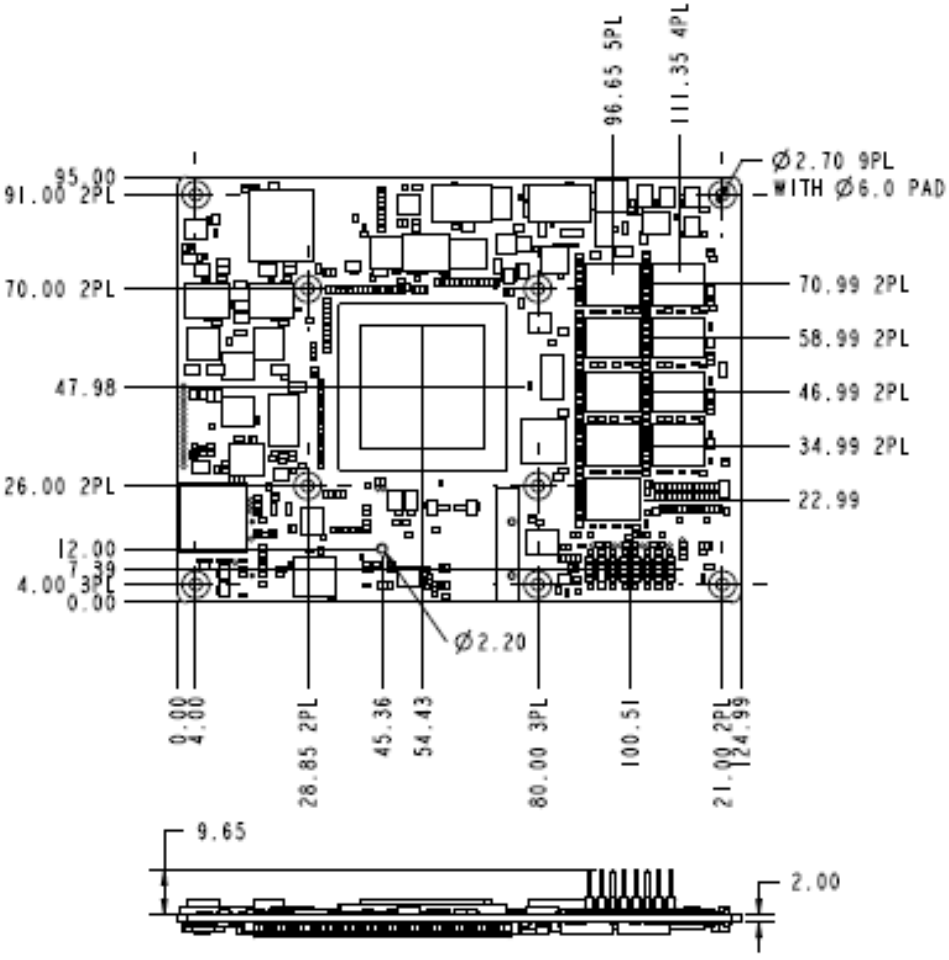


Table 1-3 COMX-P4040 ENP2 Module Dimensions

Characteristic	Value
Length	125 mm
Width	95 mm
Thickness	2 mm
Mounting height top side (component side 1)	9.65 mm

1.4 Ordering Information

Use the order numbers below when ordering product variants.

Table 1-4 Ordering Information

Order Number	Description
COMX-P4080-2G-ENP2	QorIQ P4080 with 2GB DDR3, 0 Gigabit Ethernet, 5 USB ports. COM Express Basic size.
COMX-P4080-4G-E-ENP2	QorIQ P4080 with 4GB DDR3, 1 Gigabit Ethernet, 4 USB ports. COM Express Basic Size.
COMX-P4040-4G-ENP2	QorIQ P4040 with 4GB DDR3, 1 Gigabit Ethernet, 4 USB ports. COM Express Basic Size.
COMX-CAR-P1	Artesyn DEVELOPMENT CARRIER FOR QORIQ MODULES.
COMX-P4000-ENP-HTSNK	Heatsink for COMX-P40x0 ENP2 module.

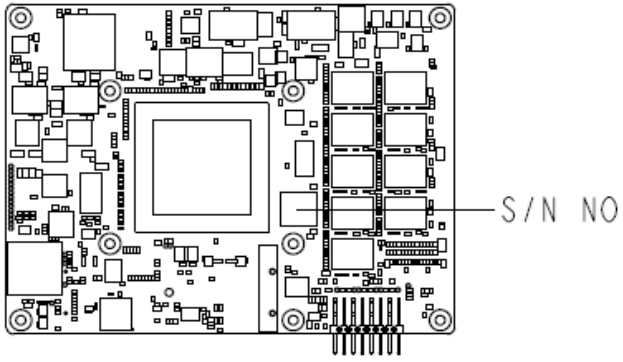
1.5 Product Identification

This section provides the serial number and its location on the COMX-P4080 ENP2 and COMX-P4040 ENP2 modules.

1.5.1 COMX-P4080 ENP2

The following figure shows the location of serial number on COMX-P4080 ENP2 module.

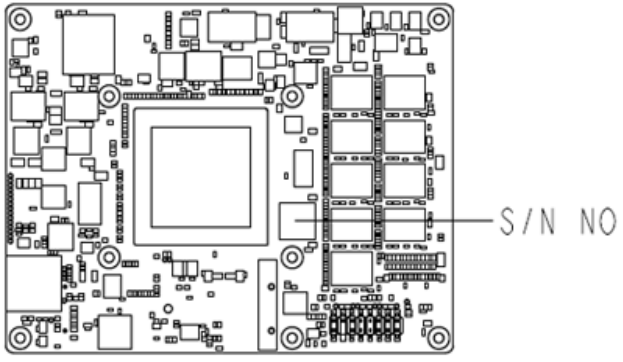
Figure 1-6 COMX-P4080 ENP2 Serial Number Location



1.5.2 COMX-P4040 ENP2

The following figure shows the location of serial number on COMX-P4040 ENP2 module.

Figure 1-7 COMX-P4040 ENP2 Serial Number Location



2.1 Environmental and Power Requirements

2.1.1 Environmental Requirements

The following environmental requirements must not be exceeded.

Operating temperature refers to the temperature of the air circulating around the module and not the component temperature.

The following table provides the environmental requirements for the module.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Temperature	-40°C to +71°C	-50°C to +100°C
Humidity	to 100% RH	to 100% RH
Vibration Sine (10mins/axis)	5 G, 15 to 2000Hz	
Vibration Random (1hr/axis)	0.04 g^2/Hz, 15 to 2000 Hz (8GRMS)	
Shock	30g/11 mS(half sine)	
Altitude	-60 to 4000 m ASL	

Thermal Requirements

A standard passive heat sink can be provided by Artesyn; 12 CFM system airflow volume (at 71°C) is needed for the heat sink to keep sufficient cooling to the module. Contact your Artesyn sales representative for detailed thermal information.

The following table summarizes the components that exhibited significant temperature rises and their maximum allowable operating temperature. These components should be monitored in order to assess thermal performance during customized thermal solution development.

Table 2-2 Critical Temperature Spots

Component Identifier	Heat Dissipation Power (W)	Maximum Allowable Temperature (°C)
CPU: P4080	20.5	CPU: 105 (Tj)
CPU: P4040	16.8	CPU: 105 (Tj)
Memory SDRAM	3	95 (Tc)
GbE Transceiver: BCM5482	0.86	125 (Tj)
Row 4, Note: For modules with Gigabit Ethernet port options.		

NOTICE

System Overheating
Improper cooling can lead to system damage and void the manufacturer's warranty.

⚠ CAUTION

Personal Injury
During operation, hot surfaces may be present on the heat sinks and the components of the product.
To prevent injury, do not touch any of the exposed components or heatsinks on the product when handling.

Power Requirements

This module is designed to operate with the input voltages and currents as defined in the following tables.

Table 2-3 Current

State	12v	VCC_RTC
Idle	2.81 A	100 uA
Full Loading (Linux)	2.91 A	100 uA

Table 2-4 COMX-P4080-4G-E-ENP2

Volts	Amps	Power
12	2.6	31.2
Total Power dissipation (W)		31.2

2.2 Unpacking and Inspecting the Enclosure

Read all notices and cautions prior to unpacking the product.

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect installation/removal of the product can damage circuits or shorten their life.
- Before touching the product make sure that you are working in an ESD-safe environment with protective equipment such an ESD wrist strap and ESD shoes. Hold the product by its edges and do not touch any components or circuits.

Shipment Inspection

1. Verify that you have received all items of your shipment.
   - COMX-P40x0-ENP2 Module
   - One printed copy of *Quick Start Guide*
   - One printed copy of *Safety Notes Summary*
   - Any other optional items that you ordered
2. Check for damage and report any damage or differences to customer service.
3. Remove the desiccant bag shipped together with the enclosure and dispose of it according to your country's legislation.

NOTICE
Improperly disposing of used products may harm the environment. Always dispose of used products according to your country's legislation and manufacturer's instructions.

The product is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, contact customer service immediately.

2.3 Installing and Removing the Module on the Carrier Board

Installing the COM Express module on the carrier board

1. Line up the board-to-board connector of the module assembly with the board-to-board connector of the carrier board.
2. Make sure that the inter-connectors are properly aligned and that the five standoffs on the module have contact with the top of the carrier board.

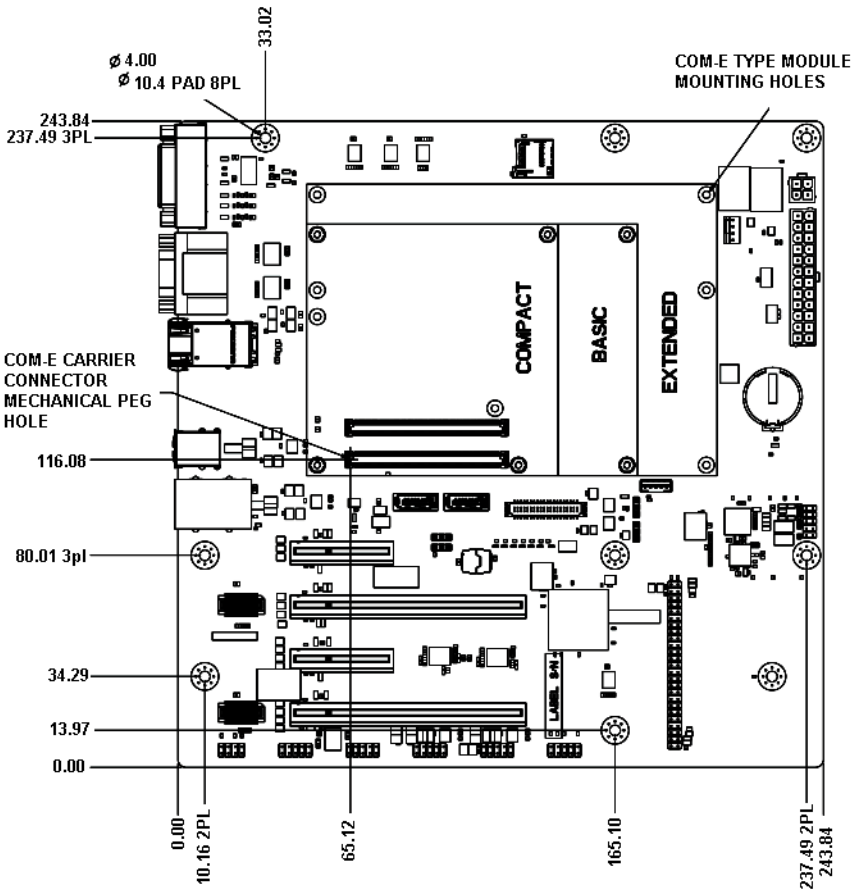
3. From the bottom side of the carrier, locate the screw holes corresponding to the module standoffs.
4. Fasten the module to the carrier board with the screws provided.

Removing the module from the carrier board

1. From the back side of the carrier, locate five screws that connect the module assembly to the carrier board.
2. Loosen and remove the screws.
3. While holding the edges, pull the module from the carrier board.

The figure below illustrates the screw-holes for mounting the module on carrier board.

Figure 2-1 Mounting Module on Carrier Board



This installation/removal procedure is only for reference. Assemble the heatsink and the module based on your own thermal solution.

Heat-sink Installation

Note: Be sure to follow the manufacturer's direction for proper heatsink/heatspreader installation and any other cooling instructions from the manufacturer.

The following figures illustrate the heat-sink installation on the module:

Figure 2-2 Heat-sink installation

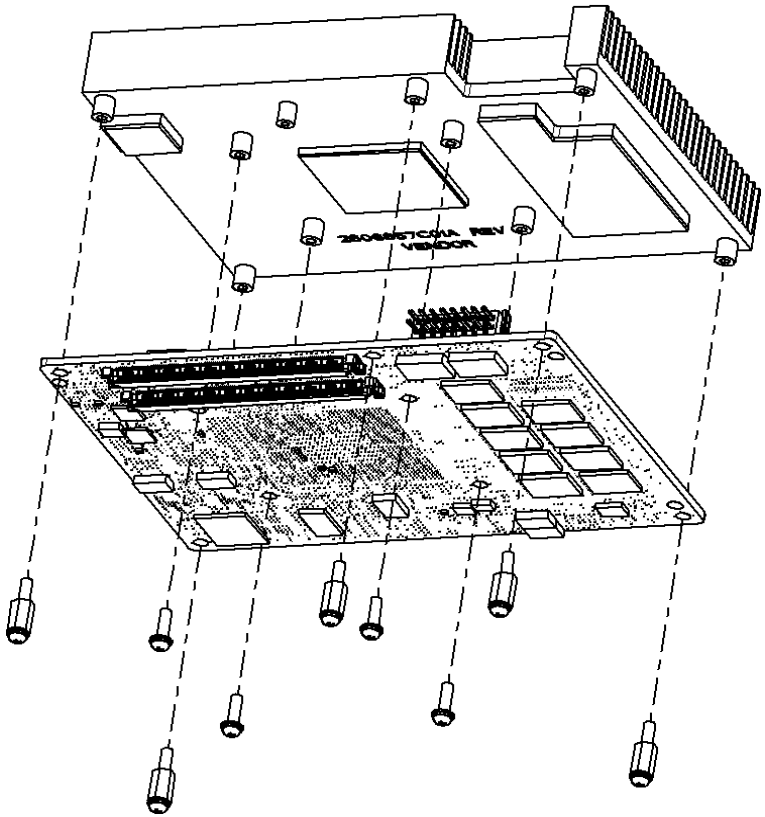
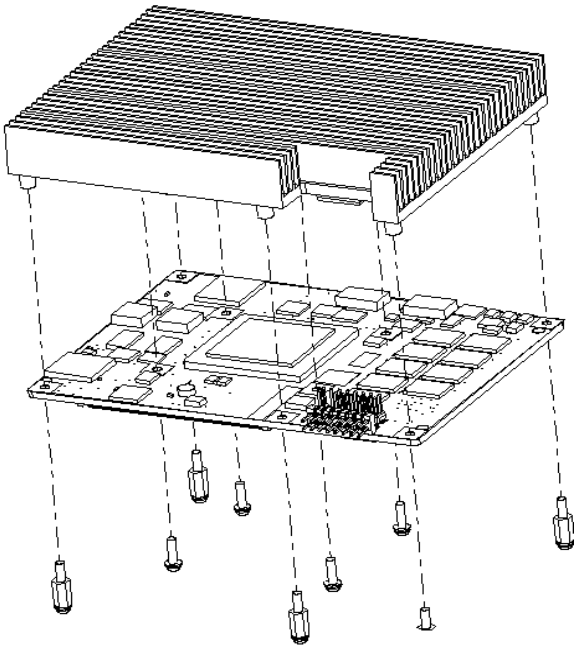


Figure 2-2 Heat-sink installation (continued)



3.1 Connectors and Switches

3.1.1 On-Board Connectors

P4080 COP Header

The following table lists the pinout of the COP (Common On-Chip Processor) header for modules with the P4080 CPU.

Table 3-1 P4080 COP Header Pinout

Pin	Signal Name
1	GND
2	cpu_ckstp_out_n
3	key for p4040 cop nc for P4080
4	cop_hrst_n
5	empty
6	cop_srst_n
7	NC
8	TMS
9	NC (CKSTP INPUT)
10	TCK
11	VDDSENSE (+3.3V)
12	NC (RUNSTOP)
13	TRST#
14	cpujtag_tdi
15	empty 10k pullup
16	cpujtag_tdo

P4040 COP Header

The following table lists the pinout of the COP header for modules with the P4040 CPU.

Table 3-2 P4040 COP Header Pinout

Pin	Signal Name
1	cpujtag_tdo
2	empty 10k pullup
3	cpujtag_tdi
4	TRST#
5	NC (RUNSTOP)
6	VDDSENSE (+3.3V)
7	TCK
8	NC (CKSTP INPUT)
9	TMS
10	NC
11	cop_srst_n
12	empty
13	cop_hrst_n
14	key for p4040 cop nc for P4080
15	cpu_ckstp_out_n
16	GND

3.1.2 ON-BOARD LEDS

There are several status LEDs provided on the module. The following table lists the LED functions.

Table 3-3 Module LED Status

LED	Status
D17	Thermal issue
D18~D19	Debug LED 1~2
D3	System asleep
D7	DDR3 power OK
D4	3.3 V power OK
D5	2.5 V power OK
D6	1.8 V power OK
D13	CORE power OK
D9	PLATFORM power OK
D10	1.5 V power OK
D15	USB hub 2 active
D16	USB hub 2 high speed
D1, D2, D15, D16 are for modules with USB port options.	

3.1.3 COMX AB-CD Connectors

The following table lists the pinout of the AB- CD COMX connectors for the P40x0 COMX modules:

Table 3-4 COMX AB-CD Connectors

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB1	A1	GND		
J2	AB1	A2	LAN1_MDI_N<3>	bidir	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB1	A3	LAN1_MDI_P<3>	bidir	
J2	AB1	A4	LAN1_LINK100_N	out	Lan1 link 100 active low
J2	AB1	A5	LAN1_LINK1000_N	out	lan1 link 1000 active low
J2	AB1	A6	LAN1_MDI_N<2	bidir	
J2	AB1	A7	LAN1_MDI_P<2	bidir	
J2	AB1	A8	LAN1_LINK_N	out	out from comx
J2	AB1	A9	LAN1_MDI_N<1>	bidir	
J2	AB1	A10	LAN1_MDI_P<1>	bidir	
J2	AB1	A11	GND		
J2	AB1	A12	LAN1_MDI_N<0>	bidir	
J2	AB1	A13	LAN1_MDI_P<0>	bidir	
J2	AB1	A14	V1P8_CTRL	out	out from comx 1.8v power indicator
J2	AB1	A15	N/C		
J2	AB1	A16	N/C		
J2	AB1	A17	N/C		
J2	AB1	A18	N/C		
J2	AB1	A19	N/C		
J2	AB1	A20	N/C		
J2	AB1	A21	GND		
J2	AB1	A22	N/C		
J2	AB1	A23	N/C		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB1	A24	N/C		
J2	AB1	A25	N/C		
J2	AB1	A26	N/C		
J2	AB1	A27	N/C		
J2	AB1	A28	N/C		
J2	AB1	A29	POVDD_EN_KEY	in	Power ON Enable
J2	AB1	A30	LBC_CS_KEY	in	Local Bus Control Chipselect key
J2	AB1	A31	GND		
J2	AB1	A32	N/C		
J2	AB1	A33	N/C		
J2	AB1	A34	N/C		
J2	AB1	A35	N/C		
J2	AB1	A36	N/C		
J2	AB1	A37	N/C		
J2	AB1	A38	N/C		
J2	AB1	A39	N/C		
J2	AB1	A40	N/C		
J2	AB1	A41	GND		
J2	AB1	A42	USB2_N	bidir	
J2	AB1	A43	USB2_P	bidir	
J2	AB1	A44	USB_OC_2_3_N	in	
J2	AB1	A45	USB0_N	bidir	
J2	AB1	A46	USB0_P	bidir	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB1	A47	V3P3_BAT		3.3v battery power
J2	AB1	A48	USB2_PWREN	out	
J2	AB1	A49	USB0_PWREN	out	
J2	AB1	A50	USB5_PWREN	out	
J2	AB1	A51	GND		
J2	AB1	A52	SERDES_TX5_P	out	
J2	AB1	A53	SERDES_TX5_N	out	
J2	AB1	A54	CPU_SDHC_DAT0	bidir	
J2	AB1	A55	SERDES_TX4_P	out	
J2	AB1	A56	SERDES_TX4_N	out	
J2	AB1	A57	GND		
J2	AB1	A58	SERDES_TX3_P	out	
J2	AB1	A59	SERDES_TX3_N	out	
J2	AB1	A60	GND		
J2	AB1	B1	GND		
J2	AB1	B2	LAN1_ACTIVITY_N	out	lan1 activity
J2	AB1	B3	TSEC_1588_CLK_OUT	out	
J2	AB1	B4	TSEC_1588_PULSE_OUT1	out	
J2	AB1	B5	TSEC_1588_PULSE_OUT2	out	
J2	AB1	B6	TSEC_1588_ALARM_OUT1	out	
J2	AB1	B7	TSEC_1588_ALARM_OUT2	out	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB1	B8	TSEC_1588_TRIG_IN 1	in	
J2	AB1	B9	TSEC_1588_TRIG_IN 2	in	
J2	AB1	B10	TSEC_1588_CLK_IN1	in	
J2	AB1	B11	GND		
J2	AB1	B12	N/C		
J2	AB1	B13	N/C		
J2	AB1	B14	N/C		
J2	AB1	B15	N/C		
J2	AB1	B16	N/C		
J2	AB1	B17	N/C		
J2	AB1	B18	N/C		
J2	AB1	B19	N/C		
J2	AB1	B20	N/C		
J2	AB1	B21	GND		
J2	AB1	B22	N/C		
J2	AB1	B23	N/C		
J2	AB1	B24	N/C		
J2	AB1	B25	N/C		
J2	AB1	B26	N/C		
J2	AB1	B27	WDT_OUT_N	out	Watch dog Timer Out
J2	AB1	B28	LBC_WE1_N	out	P40x0 local bus LWE1_N
J2	AB1	B29	N/C		
J2	AB1	B30	N/C		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB1	B31	GND		
J2	AB1	B32	LBC_LGPL5	in	
J2	AB1	B33	CPU_IIC1_CLK	bidir	
J2	AB1	B34	CPU_IIC1_DAT	bidir	
J2	AB1	B35	N/C		
J2	AB1	B36	N/C		
J2	AB1	B37	N/C		
J2	AB1	B38	USB_OC_4_5_N	in	
J2	AB1	B39	USB5_N	bidir	
J2	AB1	B40	USB5_P	bidir	
J2	AB1	B41	GND		
J2	AB1	B42	USB3_N	bidir	
J2	AB1	B43	USB3_P	bidir	
J2	AB1	B44	USB_OC_0_1_N	in	
J2	AB1	B45	USB1_N	bidir	
J2	AB1	B46	USB1_P	bidir	
J2	AB1	B47	USB3_PWREN	out	
J2	AB1	B48	USB1_PWREN	out	
J2	AB1	B49	RESET_BUTTON_N	in	
J2	AB1	B50	CB_RESET_GPIO20_N	out	
J2	AB1	B51	GND		
J2	AB1	B52	SERDES_RX5_P	in	
J2	AB1	B53	SERDES_RX5_N	in	
J2	AB1	B54	CPU_SDHC_CMD	bidir	
J2	AB1	B55	SERDES_RX4_P	in	
J2	AB1	B56	SERDES_RX4_N	in	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB1	B57	CPU_SDHC_WP	in	
J2	AB1	B58	SERDES_RX3_P	in	
J2	AB1	B59	SERDES_RX3_N	in	
J2	AB1	B60	GND		
J2	AB2	A61	SERDES_TX2_P	out	
J2	AB2	A62	SERDES_TX2_N	out	
J2	AB2	A63	CPU_SDHC_DAT1	bidir	
J2	AB2	A64	SERDES_TX1_P	out	
J2	AB2	A65	SERDES_TX1_N	out	
J2	AB2	A66	GND		
J2	AB2	A67	CPU_SDHC_DAT2	bidir	
J2	AB2	A68	SERDES_TX0_P	out	
J2	AB2	A69	SERDES_TX0_N	out	
J2	AB2	A70	GND		
J2	AB2	A71	N/C		
J2	AB2	A72	N/C		
J2	AB2	A73	N/C		
J2	AB2	A74	N/C		
J2	AB2	A75	N/C		
J2	AB2	A76	N/C		
J2	AB2	A77	N/C		
J2	AB2	A78	N/C		
J2	AB2	A79	N/C		
J2	AB2	A80	GND		
J2	AB2	A81	N/C		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB2	A82	N/C		
J2	AB2	A83	CPU_IIC2_CLK	bidir	
J2	AB2	A84	CPU_IIC2_DAT	bidir	
J2	AB2	A85	CPU_SDHC_DAT3	bidir	
J2	AB2	A86	N/C		
J2	AB2	A87	N/C		
J2	AB2	A88	CLK_125M_100M_COME_SDREF1_P	out	
J2	AB2	A89	CLK_125M_100M_COME_SDREF1_N	out	
J2	AB2	A90	GND		
J2	AB2	A91	CPU_SPI_CS0_K_N	out	
J2	AB2	A92	CPU_SPI_MISO	in	
J2	AB2	A93	CPU_SDHC_CLK	out	
J2	AB2	A94	CPU_SPI_CLK_COME	out	
J2	AB2	A95	CPU_SPI_MOSI	out	
J2	AB2	A96	GND		
J2	AB2	A97	V12		
J2	AB2	A98	V12		
J2	AB2	A99	V12		
J2	AB2	A100	GND		
J2	AB2	A101	V12		
J2	AB2	A102	V12		
J2	AB2	A103	V12		
J2	AB2	A104	V12		
J2	AB2	A105	V12		
J2	AB2	A106	V12		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB2	A107	V12		
J2	AB2	A108	V12		
J2	AB2	A109	V12		
J2	AB2	A110	GND		
J2	AB2	B61	SERDES_RX2_P	in	
J2	AB2	B62	SERDES_RX2_N	in	
J2	AB2	B63	CPU_SDHC_CD	bi	
J2	AB2	B64	SERDES_RX1_P	in	
J2	AB2	B65	SERDES_RX1_N	in	
J2	AB2	B66	N/C		
J2	AB2	B67	CPU_HRESET_COME_N	in	Only used on P4080-2G assembly
J2	AB2	B68	SERDES_RX0_P	in	
J2	AB2	B69	SERDES_RX0_N	in	
J2	AB2	B70	GND		
J2	AB2	B71	N/C		
J2	AB2	B72	N/C		
J2	AB2	B73	N/C		
J2	AB2	B74	N/C		
J2	AB2	B75	N/C		
J2	AB2	B76	N/C		
J2	AB2	B77	N/C		
J2	AB2	B78	N/C		
J2	AB2	B79	N/C		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB2	B80	GND		
J2	AB2	B81	N/C		
J2	AB2	B82	N/C		
J2	AB2	B83	N/C		
J2	AB2	B84	V5SB		
J2	AB2	B85	V5SB		
J2	AB2	B86	V5SB		
J2	AB2	B87	V5SB		
J2	AB2	B88	CPU_SPI_CS1_N	out	
J2	AB2	B89	N/C		
J2	AB2	B90	GND		
J2	AB2	B91	N/C		
J2	AB2	B92	N/C		
J2	AB2	B93	N/C		
J2	AB2	B94	N/C		
J2	AB2	B95	CPU_IIC4_CLK	bidir	
J2	AB2	B96	CPU_IIC4_DAT	bidir	
J2	AB2	B97	BANK1_SEL_FS0	in	
J2	AB2	B98	BANK2_SEL_S1	in	
J2	AB2	B99	BANK3_SEL_S1	in	
J2	AB2	B100	GND		
J2	AB2	B101	V12		
J2	AB2	B102	V12		
J2	AB2	B103	V12		
J2	AB2	B104	V12		
J2	AB2	B104	V12		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J2	AB2	B106	V12		
J2	AB2	B107	V12		
J2	AB2	B108	V12		
J2	AB2	B109	V12		
J2	AB2	B110	GND		
J3	CD1	A1	GND		
J3	CD1	A2	LAN2_ACTIVITY_N	in	
J3	CD1	A3	LAN2_MDI_N<3>	bidir	
J3	CD1	A4	LAN2_MDI_P<3>	bidir	
J3	CD1	A5	LAN2_LINK100_N	in	
J3	CD1	A6	LAN2_MDI_N<2>	bidir	
J3	CD1	A7	LAN2_MDI_P<2>	bidir	
J3	CD1	A8	LAN2_LINK1000_N	in	
J3	CD1	A9	LAN2_MDI_N<1>	bidir	
J3	CD1	A10	LAN2_MDI_P<1>	bidir	
J3	CD1	A11	GND		
J3	CD1	A12	LAN2_MDI_N<0>	bidir	
J3	CD1	A13	LAN2_MDI_P<0>	bidir	
J3	CD1	A14	LAN2_LINK_N	in	
J3	CD1	A15	LBC_LAD<8>	bidir	
J3	CD1	A16	LBC_LAD<9>	bidir	
J3	CD1	A17	LBC_CLE_N	out	
J3	CD1	A18	LBC_FCMALE_N	out	
J3	CD1	A19	SERDES_RX6_P	in	
J3	CD1	A20	SERDES_RX6_N	in	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD1	A21	GND		
J3	CD1	A22	SERDES_RX7_P	in	
J3	CD1	A23	SERDES_RX7_N	in	
J3	CD1	A24	N/C		
J3	CD1	A25	LBC_LAD<10>	bidir	
J3	CD1	A26	LBC_LAD<11>	bidir	
J3	CD1	A27	LBC_LAD<12>	bidir	
J3	CD1	A28	LBC_LAD<13>	bidir	
J3	CD1	A29	LBC_LAD<14>	bidir	
J3	CD1	A30	LBC_LAD<15>	bidir	
J3	CD1	A31	GND		
J3	CD1	A32	CPU_UART1_SOUT	out	
J3	CD1	A33	CPU_UART1_SIN	in	
J3	CD1	A34	CPU_UART1_CTS	out	Not used
J3	CD1	A35	CPU_UART1_RTS	in	Not used
J3	CD1	A36	CPU_UART2_SOUT	out	
J3	CD1	A37	CPU_UART2_SIN	in	
J3	CD1	A38	CPU_UART2_CTS	out	Not used
J3	CD1	A39	CPU_UART2_RTS	in	Not used
J3	CD1	A40	EMI1_MDIO	bidir	
J3	CD1	A41	GND		
J3	CD1	A42	CPU_UART3_SOUT	out	
J3	CD1	A43	CPU_UART3_SIN	in	
J3	CD1	A44	N/C		
J3	CD1	A45	N/C		
J3	CD1	A46	CPU_UART4_SOUT	out	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD1	A47	CPU_UART4_SIN	in	
J3	CD1	A48	N/C		
J3	CD1	A49	N/C		
J3	CD1	A50	EMI1_MDC_COME	out	
J3	CD1	A51	GND		
J3	CD1	A52	SERDES_RX16_P	in	
J3	CD1	A53	SERDES_RX16_N	in	
J3	CD1	A54	COME_TYPE0_N	out	
J3	CD1	A55	SERDES_RX17_P	in	
J3	CD1	A56	SERDES_RX17_N	in	
J3	CD1	A57	COME_TYPE1_N	out	
J3	CD1	A58	SERDES_RX18_P	in	
J3	CD1	A59	SERDES_RX18_N	in	
J3	CD1	A60	GND		
J3	CD1	B1	GND		
J3	CD1	B2	N/C		
J3	CD1	B3	N/C		
J3	CD1	B4	N/C		
J3	CD1	B5	N/C		
J3	CD1	B6	N/C		
J3	CD1	B7	N/C		
J3	CD1	B8	N/C		
J3	CD1	B9	N/C		
J3	CD1	B10	N/C		
J3	CD1	B11	GND		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD1	B12	N/C		
J3	CD1	B13	N/C		
J3	CD1	B14	N/C		
J3	CD1	B15	CPU_IRQ_OUT	out	
J3	CD1	B16	CPU_IRQ0	in	
J3	CD1	B17	LBC_CLK0	out	
J3	CD1	B18	LBC_CLK1	out	
J3	CD1	B19	SERDES_TX6_P	out	
J3	CD1	B20	SERDES_TX6_N	out	
J3	CD1	B21	GND		
J3	CD1	B22	SERDES_TX7_P	out	
J3	CD1	B23	SERDES_TX7_N	out	
J3	CD1	B24	LBC_CS6_N	out	
J3	CD1	B25	LBC_CS3_N	out	
J3	CD1	B26	LBC_LA<31>	bidir	
J3	CD1	B27	LBC_LA<30>	bidir	
J3	CD1	B28	LBC_LAD<0>	bidir	
J3	CD1	B29	LBC_LA<29>	bidir	
J3	CD1	B30	LBC_LA<28>	bidir	
J3	CD1	B31	GND		
J3	CD1	B32	LBC_LA<27>	bidir	
J3	CD1	B33	LBC_LA<26>	bidir	
J3	CD1	B34	LBC_LAD<1>	bidir	
J3	CD1	B35	LBC_LAD<2>	bidir	
J3	CD1	B36	LBC_LA<25>	bidir	
J3	CD1	B37	LBC_LA<24>	bidir	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD1	B38	LBC_LA<23>	bidir	
J3	CD1	B39	LBC_LA<22>	bidir	
J3	CD1	B40	LBC_LA<21>	bidir	
J3	CD1	B41	GND		
J3	CD1	B42	LBC_LA<20>	bidir	
J3	CD1	B43	LBC_LA<19>	bidir	
J3	CD1	B44	LBC_LA<18>	bidir	
J3	CD1	B45	LBC_LAD<3>	bidir	
J3	CD1	B46	LBC_LAD<4>	bidir	
J3	CD1	B47	LBC_LAD<5>	bidir	
J3	CD1	B48	LBC_LAD<6>	bidir	
J3	CD1	B49	LBC_LAD<7>	bidir	
J3	CD1	B50	LBC_ALE_N	out	
J3	CD1	B51	GND		
J3	CD1	B52	SERDES_TX16_P	out	
J3	CD1	B53	SERDES_TX16_N	out	
J3	CD1	B54	COME_TYPE3_N	out	
J3	CD1	B55	SERDES_TX17_P	out	
J3	CD1	B56	SERDES_TX17_N	out	
J3	CD1	B57	COME_TYPE2_N	out	
J3	CD1	B58	SERDES_TX18_P	out	
J3	CD1	B59	SERDES_TX18_N	out	
J3	CD1	B60	GND		
J3	CD2	A61	SERDES_RX19_P	in	
J3	CD2	A62	SERDES_RX19_N	in	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD2	A63	CPU_EMI2_MDIO	bidir	
J3	CD2	A64	GND		
J3	CD2	A65	SERDES_RX20_P	in	
J3	CD2	A66	SERDES_RX20_N	in	
J3	CD2	A67	LBC_CS5_N	out	
J3	CD2	A68	SERDES_RX21_P	in	
J3	CD2	A69	SERDES_RX21_N	in	
J3	CD2	A70	GND		
J3	CD2	A71	SERDES_RX22_SATA 1_P	in	
J3	CD2	A72	SERDES_RX22_SATA 1_N	in	
J3	CD2	A73	N/C		
J3	CD2	A74	SERDES_RX23_SATA 2_P	in	
J3	CD2	A75	SERDES_RX23_SATA 2_N	in	
J3	CD2	A76	N/C		
J3	CD2	A77	LBC_OE_N	out	
J3	CD2	A78	N/C		
J3	CD2	A79	N/C		
J3	CD2	A80	GND		
J3	CD2	A81	LBC_WP_N	out	
J3	CD2	A82	LBC_RB_N	out	
J3	CD2	A83	CPU_IRQ1	in	
J3	CD2	A84	GND		
J3	CD2	A85	CPU_IRQ2	in	
J3	CD2	A86	CPU_IRQ3	in	

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD2	A87	GND		
J3	CD2	A88	CPU_GPI0	in	
J3	CD2	A89	CPU_GPI1	in	
J3	CD2	A90	GND		
J3	CD2	A91	IOEXT_GPI5	in	
J3	CD2	A92	CPU_GPI3	in	
J3	CD2	A93	GND		
J3	CD2	A94	CPU_GPI4	in	
J3	CD2	A95	IOEXT_GPI6	in	
J3	CD2	A96	GND		
J3	CD2	A97	IOEXT_GPI7	in	
J3	CD2	A98	CPU_SPI_CS2_N	out	
J3	CD2	A99	CPU_SPI_CS3_N	out	
J3	CD2	A100	GND		
J3	CD2	A101	CLK_125M_100M_COME_SDREF2_P	out	
J3	CD2	A102	CLK_125M_100M_COME_SDREF2_N	out	
J3	CD2	A103	GND		
J3	CD2	A104	V12		
J3	CD2	A105	V12		
J3	CD2	A106	V12		
J3	CD2	A107	V12		
J3	CD2	A108	V12		
J3	CD2	A109	V12		
J3	CD2	A110	GND		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD2	B61	SERDES_TX19_P	out	
J3	CD2	B62	SERDES_TX19_N	out	
J3	CD2	B63	CPU_EMI2_MDC	out	
J3	CD2	B64	LP_TMP_DET_BAT	out	
J3	CD2	B65	SERDES_TX20_P	out	
J3	CD2	B66	SERDES_TX20_N	out	
J3	CD2	B67	GND		
J3	CD2	B68	SERDES_TX21_P	out	
J3	CD2	B69	SERDES_TX21_N	out	
J3	CD2	B70	GND		
J3	CD2	B71	SERDES_TX22_SATA 1_P	out	
J3	CD2	B72	SERDES_TX22_SATA 1_N	out	
J3	CD2	B73	N/C		
J3	CD2	B74	SERDES_TX23_SATA 2_P	out	
J3	CD2	B75	SERDES_TX23_SATA 2_N	out	
J3	CD2	B76	GND		
J3	CD2	B77	LBC_WE0_N	out	
J3	CD2	B78	LBC_LA<16>	bi	
J3	CD2	B79	LBC_LA<17>	bi	
J3	CD2	B80	GND		
J3	CD2	B81	LBC_CTL_N	out	
J3	CD2	B82	LBC_CS4_N	out	
J3	CD2	B83	CPU_IRQ4	in	
J3	CD2	B84	GND		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD2	B85	IOEXT_GPI8	in	
J3	CD2	B86	N/C		
J3	CD2	B87	GND		
J3	CD2	B88	CPU_GPO0	out	
J3	CD2	B89	CPU_GPO1	out	
J3	CD2	B90	GND		
J3	CD2	B91	IOEXT_GPO5	out	
J3	CD2	B92	CPU_GPO3	out	
J3	CD2	B93	GND		
J3	CD2	B94	CPU_GPO4	out	
J3	CD2	B95	IOEXT_GPO6	out	
J3	CD2	B96	GND		
J3	CD2	B97	CPU_TMP_DETECT_N	in	cpu temp detect
J3	CD2	B98	N/C		
J3	CD2	B99	N/C		
J3	CD2	B100	GND		
J3	CD2	B101	P50_LP_TMP_DETECT_GPO7	out	
J3	CD2	B102	IOEXT_GPO8	out	
J3	CD2	B103	GND		
J3	CD2	B104	V12		
J3	CD2	B105	V12		
J3	CD2	B106	V12		
J3	CD2	B107	V12		
J3	CD2	B108	V12		
J3	CD2	B109	V12		

Table 3-4 COMX AB-CD Connectors (continued)

Connector ref	Connector name	Pin	Net Name	Direction from COMX	Notes
J3	CD2	B110	GND		

Functional Description

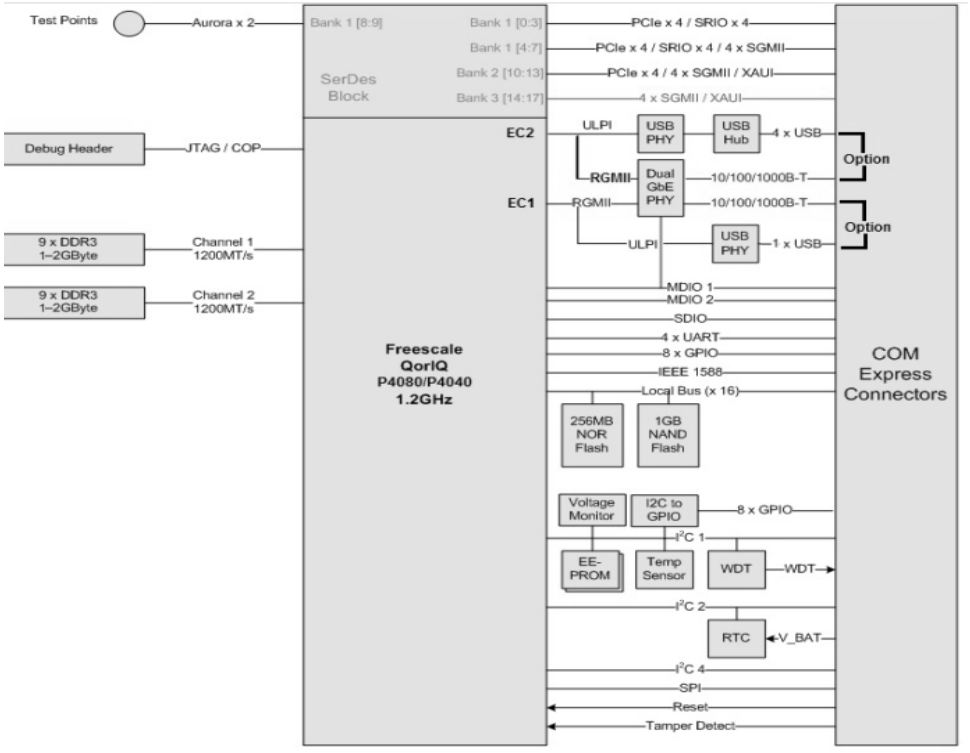
4.1 Overview

The COMX-P40x0 ENP2 is a COM Express module based on the Freescale QorIQ™ P4040/P4080 processors. This module provides some of the universal interfaces such as Gigabit Ethernet, USB, PCIE, and so on. This module is designed to support the processor at 1.2 GHz core frequency. Currently productized variants support up to 4 GB of DDR3 soldered down.

The QorIQ P4080 integrated communication processor has eight processor cores while the P4040 has four processor cores. The processors provides high-performance data path acceleration logic, network and peripheral bus interfaces required for networking, telecommunication, data communication, wireless infrastructure, and military/aerospace applications.

4.2 Block Diagram

Figure 4-1 COMX-P40x0 ENP2 Block Diagram



4.3 Processor Core and Cache Memory Complex

The QorIQ P4080/P4040 processor has eight/four high-performance 32-bit Power Architecture Book E-compliant e500mc cores. Each e500mc is a superscalar dual issue processor that supports out-of-order execution and in-order completion, thus making it perform better than other RISC and CISC architectures.

Features of e500mc

- 36-bit physical addressing
- 512-entry 4 KB pages
- 3 Integer units (2 simple, 1 complex)
- 1.2 GHz at 1.0V
- 64 Byte cache line size
- L1 caches
- User, Supervisor, and Hypervisor instruction level privileges
- APU, classic double precision floating point unit
- 128 KB private L2 cache running at the same frequency of CPU
- 2 MB of shared L3 CoreNet platform cache (CPC)

4.4 Integrated Memory Controller

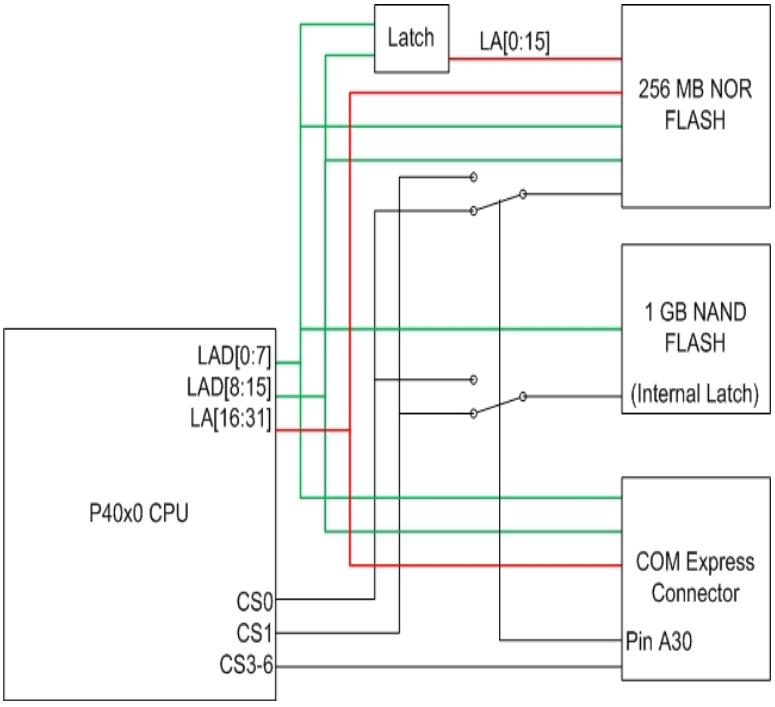
The P4080/P4040 processor integrates two DDR controllers that support DDR2 and DDR3 SDRAM. It can support a maximum of 64 GB of main memory. ENP2 modules are limited to 8 GB, using 4 Gb devices.The ECC capability detects all double-bit errors, detects all multi-bit errors within a nibble, and corrects all single-bit errors. The DDR controller is capable of self-refresh mode and an initialization bypass during system power-on after an abnormal shutdown for use by designers in preventing re-initialization.

4.5 Local Bus

The 16-bit wide local bus is connected to a 2 Gb or 256 MB NOR Flash and an 8 Gb or 1 GB NAND FLASH. The NOR FLASH is used to store the RCW data (active and alternates), FMan microcode, DTB, U-Boot, demo Linux kernel and associated basic ramdisk. By default, the NAND FLASH is used to store an alternate Linux file system. The local bus is also extended to the COM Express connectors. There are six chip select signals supported - CS0, CS1 and CS3-6. CS0 is reserved for the boot device and defaults to the NOR FLASH. CS1 defaults to the NAND FLASH. CS0 and CS1 can be swapped between the NOR and NAND FLASH by driving the COM Express connector pin A30 high (+3.3 V). CS3-6 are extended to the COM Express connector and are available for use.

The following figure illustrates the distribution of local bus on the module:

Figure 4-2 Distribution of Local Bus on P40x0



4.5.1 Clock

The eLBC clock is generated by platform clock. The divisor is configured by CLKDIV in Clock Ratio Register (LCRR). The clock is limited to 75 MHz maximum frequency.

4.5.2 NOR FLASH

The NOR FLASH is attached to the GPCM on the local bus and operates in 16-bit mode.

The NOR FLASH is a Micron PC28F00BM29EWHA. Its size is 2 Gb/ 256 MB. It has 2048 uniform blocks, 128 KB or 64 K words each.

The physical address for the NOR FLASH is 0xFE0000000 - 0xFEFFFFFFF.

The NOR FLASH contains RCW data, U-Boot image, U-Boot environment variables, kernel image, device tree blob, RAMDISK image and FMAN ucode image. The detailed map is described in the following table:

Table 4-1 NOR FLASH Map

Block#	Blocks	Start	End	Size	Description
0	1	0000 0000	0001 FFFF	128 KB	Active RCW Option Data
1	1	0002 0000	0003 FFFF	128 KB	RCW Option Data 1
2	1	0004 0000	0005 FFFF	128 KB	RCW Option Data 2
3	1	0006 0000	0007 FFFF	128 KB	RCW Option Data 3
4	1	0008 0000	0009 FFFF	128 KB	RCW Option Data 4
5	1	000A 0000	000B FFFF	128 KB	RCW Option Data 5
6	1	000C 0000	000D FFFF	128 KB	RCW Option Data 6
7	1	000E 0000	000F FFFF	128 KB	RCW Option Data 7
8	1	0010 0000	0011 FFFF	128 KB	RCW Option Data 8
9	1	0012 0000	0013 FFFF	128 KB	RCW Option Data 9
10	1	0014 0000	0015 FFFF	128 KB	RCW Option Data 10
11	1	0016 0000	0017 FFFF	128 KB	RCW Option Data 11
12	1	0018 0000	0019 FFFF	128 KB	RCW Option Data 12
13	3	001A 0000	0020 0000	384KB	Not Used
16	112	0020 0000	00FF FFFF	14 MB	FMAN ucode Image
128	1792	0100 0000	0EFF FFFF	224 MB	RAMDISK Image
1920	120	0F00 0000	0FEF FFFF	15 MB	Kernel Image
2040	3	0FF0 0000	0FF5 FFFF	384 KB	Device Tree Blob
2043	1	0FF6 0000	0FF7 FFFF	128 KB	U-Boot Env Variable
2044	4	0FF8 0000	0FFF FFFF	512 KB	U-Boot Image

4.5.3 NAND FLASH

The NAND FLASH is a Micron MT29F8G08ADADAH4 with a size of 8 Gb/1 GB. Each page contains 2112 bytes including 2048 bytes of data and 64 bytes of spare. Each block contains 64 pages including 128 KB of data and 4 KB of spare. There are a total of 8192 blocks.

As shipped, the NAND FLASH is only used as NAND FLASH JFFS2 rootfs. The map is described as below table:

Table 4-2 NAND FLASH Map

Start Address	End Address	Size	Description
0000 0000	00FF FFFF	16 MB	Not Used
0100 0000	3FFF FFFF	1 GB - 16 MB	NAND FLASH JFFS2 rootfs

4.6 SerDes Block

The P4040/P4080 processor provides three banks of SerDes with a total of 18 lanes. Bank 1 routes eight lanes to the COM Express connector as SerDes[0:7]. Bank 2 routes four lanes to the COM Express connector as SerDes[16:19]. Bank 3 also routes four lanes to the COM Express connector but is unused for this module. Bank 1 provides two additional SerDes lanes on-board for CPU debugging through the Aurora interface. See note in the *Overview* on page 25.

The protocol running on each lane or group of lanes routed to the COM Express connector is configured by the RCW. Available options are shown in the following table (slot numbers refer to COMX-CAR-P1 PCI Express connector slots):

Table 4-3 Options of the SerDes routed to COM Express Connectors

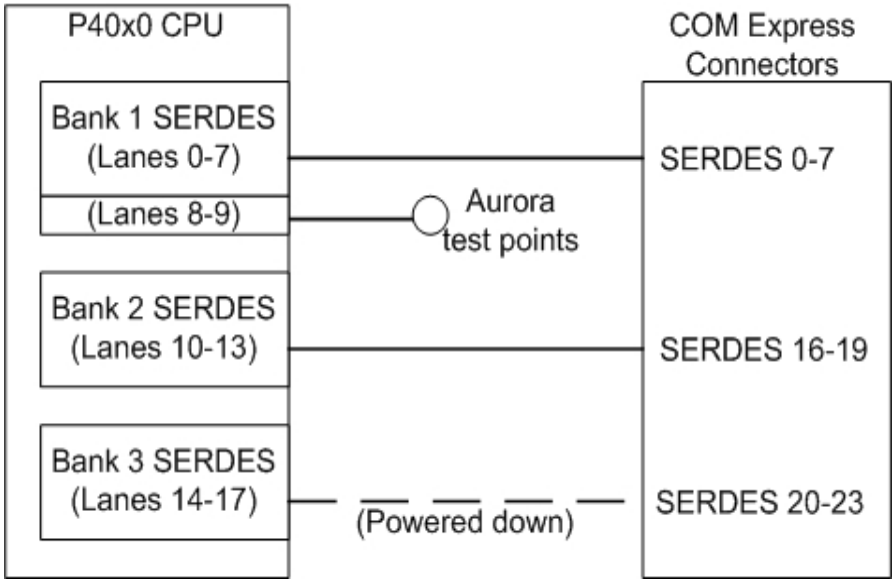
Option	Bank1 SerDes 0-3 (SLOT J6)	Bank1 SerDes 4-7 (SLOT J14)	Bank2 SerDes 10-13 (SLOT J10)	Bank3 SerDes 14-17 (Slot J2)[4]	RCW [SRDS_PRTCL]	Bank 1 SerDes Clock3	Bank 2/3 SerDes Clock3
1	PCIe1 x4 (2.5 Gbps)	PCIe2 x4 (2.5 Gbps)	XAUI FM2 (3.125 Gbps)[1]	XAUI FM1 (3.125 Gbps)[1]	0x05	100 MHz[3]	125 MHz[3]
2	PCIe1 x4 (2.5 Gbps)	PCIe2 x4 (5 Gbps)	XAUI FM2 (3.125 Gbps)[1]	XAUI FM1 (3.125 Gbps)[1]	0x05	100 MHz[3]	125 MHz[3]
3	PCIe1 x4 (5 Gbps)	PCIe2 x4 (2.5 Gbps)	XAUI FM2 (3.125 Gbps)[1]	XAUI FM1 (3.125 Gbps)[1]	0x05	100 MHz[3]	125 MHz[3]
4	PCIe1 x4 (5 Gbps)	PCIe2 x4 (5 Gbps)	XAUI FM2 (3.125 Gbps)[1]	XAUI FM1 (3.125 Gbps)[1]	0x05	100 MHz[3]	125 MHz[3]
5	PCIe1 x4 (2.5 Gbps)	SGMII FM2 x4 (1.25 Gbps)	XAUI FM2 (3.125 Gbps)[1]	Reserved[2]	0x0F	100 MHz[3]	125 MHz[3]
6	PCIe1 x4 (2.5 Gbps)	SGMII FM2 x4 (1.25 Gbps)	XAUI FM2 (3.125 Gbps)[1]	Reserved[2]	0x0F	100 MHz[3]	125 MHz[3]
7	SRIO2 x4 (3.125 Gbps)	SRIO1 x4 (3.125 Gbps)	PCIe3 x4 (2.5 Gbps)[1]	SGMII FM1 x4 (1.25 Gbps)[1]	0x19	125 MHz[3]	100 MHz[3]
8	SRIO2 x4 (3.125 Gbps)	SRIO1 x4 (3.125 Gbps)	PCIe3 x4 (5 Gbps)[1]	SGMII FM1 x4 (1.25 Gbps)[1]	0x19	125 MHz[3]	100 MHz[3]
9	SRIO2 x4 (2.5 Gbps)	SRIO1 x4 (2.5 Gbps)	XAUI FM2 (3.125 Gbps)[1]	XAUI FM1 (3.125 Gbps)[1]	0x13	100 MHz[3]	125 MHz[3]
10	SRIO2 x4 (3.125 Gbps)	SRIO1 x4 (3.125 Gbps)	SGMII FM2 x4 (1.25 Gbps)[1]	SGMII FM1 x4 (1.25 Gbps)[1]	0x16	125 MHz[3]	125 MHz[3]
11	PCIe1 x4 (2.5 Gbps)	SRIO1 x4 (2.5 Gbps)	XAUI FM2 (3.125 Gbps)[1]	XAUI FM1 (3.125 Gbps)[1]	0x22	100 MHz[3]	125 MHz[3]
12	PCIe1 x4 (5 Gbps)	SRIO1 x4 (2.5 Gbps)	XAUI FM2 (3.125 Gbps)[1]	XAUI FM1 (3.125 Gbps)[1]	0x22	100 MHz[3]	125 MHz[3]

1 SerDes Bank2 and Bank3 are powered down by default by the RCW, but are later enabled by the firmware.
2 SerDes Bank 3 is unavailable in this configuration.
3 SerDes reference clocks must be properly configured by the carrier or CPU GPIO pins for the selected interfaces to work. See Clock Structure section for clock settings.

4 Only SerDes lane 14 is routed to Slot J2.

The following figure illustrates the distribution of SerDes lanes on the module:

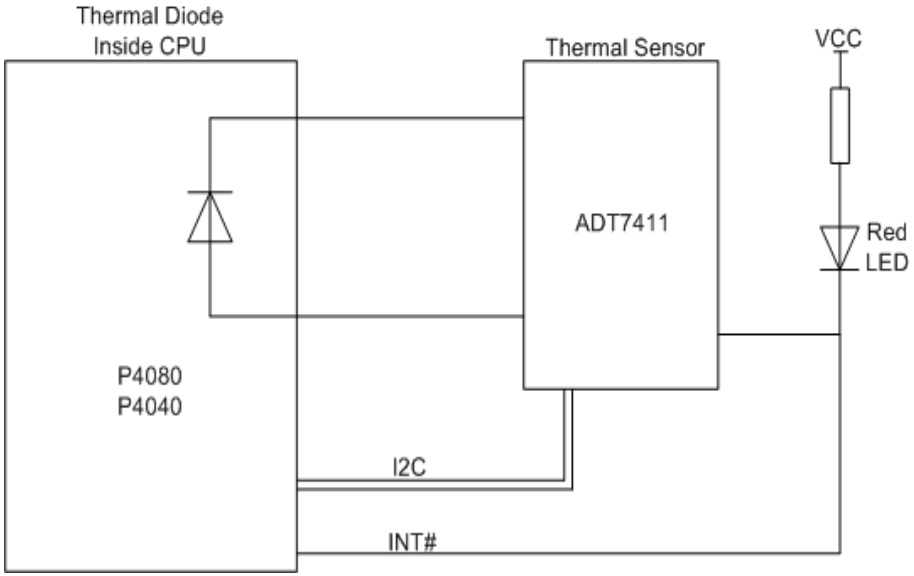
Figure 4-3 Distribution of SerDes Lanes



4.7 Thermal Management

The COMX-P40x0 ENP2 module provides a thermal management strategy. This includes CPU junction temperature monitoring as shown in the following figure:

Figure 4-4 Module Thermal Management



A thermal diode is integrated in the P40x0, which connects to a thermal sensor ADT7411. The CPU can get the junction temperature via I2C.

When the junction temperature reaches105 °C, the ADT7411 drives INT# low, to indicate an interrupt to the CPU. The red LED D17 shows the interrupt status.

LED	Definition	Status	Description
D17	INT# signal is active	ON	The CPU temperature has reached 105°C
		OFF	Normal status

4.8 Main Memory

4.8.1 Memory Interface

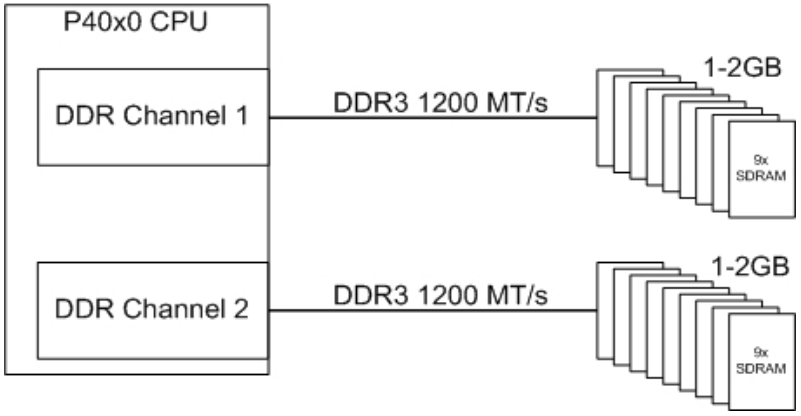
The QorIQ P40x0 processor supports two individual DDR channels that are configured for DDR3 operation at 600 MHz or 1200 MT/s. Each channel consists of 64-bit data and 8-bit ECC.

The module supports either 1 GB or 2 GB of on-board memory per channel for a total of 2 GB or 4 GB. Each memory bank consists of 9 memory chips of 8-bits with each bank located on opposite sides of the board.

The SDRAM package height is maximum of 1.2 mm.

The following figure illustrates the DDR memory architecture per controller:

Figure 4-5 Memory Interface



4.8.2 Memory Map

The following table provides the U-boot memory map of the COMX-P40x0 ENP2.

Table 4-4 Memory Map

Address#	32-bit Effective Base Address	36-bit Physical Base Address	Size	Description
1.	0000 0000	0 0000 0000	8000 0000 - 2 GB	DDR3 Memory, NOTE1
2.	8000 0000	C 0000 0000	2000 0000 - 512 MB	PCIE1 MEM
3.	A000 0000	C 2000 0000	2000 0000 - 512 MB	PCIE2 MEM, NOTE2
4.	A000 0000	C 2000 0000	1000 0000 - 256 MB	RIO1 MEM, NOTE2
5.	B000 0000	C 3000 0000	1000 0000 - 256 MB	RIO2 MEM, NOTE2
6.	C000 0000	C 4000 0000	0800 0000 - 512 MB	PCIE3 MEM
7.	E000 0000	F E000 0000	1000 0000 - 256 MB	LBC NOR FLASH
8.	F000 0000	F F000 0000	0040 0000 - 4 MB	DCSR
9.	F400 0000	F F400 0000	0020 0000 - 2 MB	BMAN MEM
10.	F420 0000	F F420 0000	0020 0000 - 2 MB	QMAN MEM
11.	F800 0000	F F800 0000	0001 0000 - 64 KB	PCIE1 IO
12.	F801 0000	F F801 0000	0001 0000 - 64 KB	PCIE2 IO
13.	F802 0000	F F802 0000	0001 0000 - 64 KB	PCIE3 IO
14.	FFA0 0000	F FFA0 0000	0010 0000 - 1 MB	NAND FLASH Buffer
15.	FE00 0000	F FE00 0000	0100 0000 - 16 MB	CCSR
16.	FFFF F000	0 FFFF F000	0000 1000 - 4 KB	BOOT PAGE

Note1: Only up to 2 GB memory is mapped in U-Boot and the other memory is left unmapped and not used if more than 2 GB memory is fitted. More than 2 GB can be used in Linux. Up to 4 GB has been verified.

Note2: Address #4 and #5 is used instead of address #3 if RIO is configured

4.9 GPIO

The COMX-P40x0-ENP2 module supports a total of 20 GPIO pins. The following table lists the GPIOs:

Table 4-5 GPIO

GPIO name	function
CPU_GPIO0	GPI0 of COM Express connectors
CPU_GPIO1	GPI1 of COM Express connectors
CPU_GPIO2	GPI3 of COM Express connectors
CPU_GPIO3	GPI4 of COM Express connectors
CPU_GPIO4	GPO0 of COM Express connectors
CPU_GPIO5	GPO1 of COM Express connectors
CPU_GPIO6	GPO3 of COM Express connectors
CPU_GPIO7	GPO4 of COM Express connectors
CPU_GPIO19	Clock generators enable control
CPU_GPIO20	Carried board reset output
CPU_GPIO23	Clock generator of bank 1 frequency selection
CPU_GPIO24	Clock generator of bank 2-3 frequency selection
IOEXT_GPI5 (PCA9557 I/O0)	GPI5 of COM Express connectors
IOEXT_GPI6 (PCA9557 I/O1)	GPI6 of COM Express connectors
IOEXT_GPI7 (PCA9557 I/O2)	GPI7 of COM Express connectors
IOEXT_GPI8 (PCA9557 I/O3)	GPI8 of COM Express connectors
IOEXT_GPO5 (PCA9557 I/O4)	GPO5 of COM Express connectors
IOEXT_GPO6 (PCA9557 I/O5)	GPO6 of COM Express connectors

Table 4-5 GPIO

GPIO name	function
IOEXT_GPO7 (PCA9557 I/O6)	GPO7 of COM Express connectors
IOEXT_GPO8 (PCA9557 I/O7)	GPO8 of COM Express connectors

GPIO19, 20, 23, and 24 are multiplexed with other functional blocks. The pins should be configured as follows.

GPIO19: RCW [DMA1]=1b

GPIO20: RCW [DMA2]=10b

GPIO23/24: RCW [IRQ]=1b

After reset, the direction for all GPIOs are set to input. All GPIOs used as output need to be reconfigured.

Figure 4-6 Distribution of GPIO

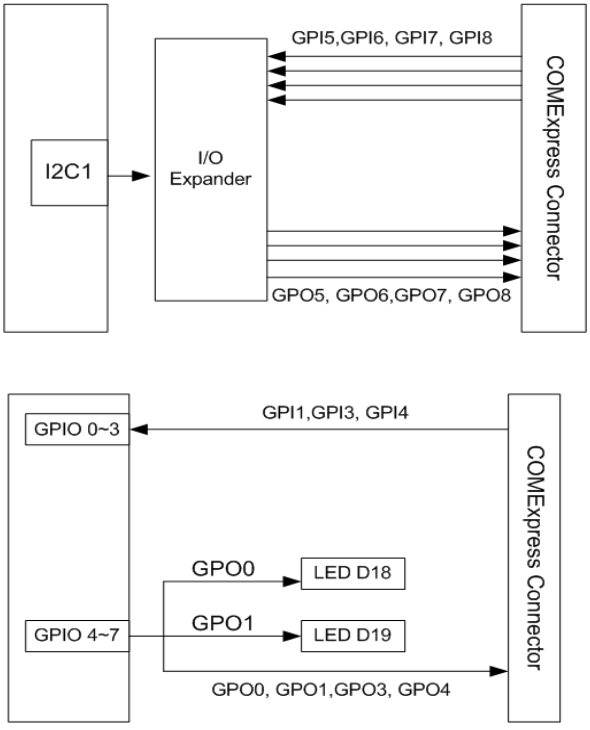


Table 4-6 GPIO

PCA955NAME - GPIO NAME	COMX PLUG.PIN
IO0 - GPI5	CD.A91
IO1 - GPI6	CD.A95
IO2 - GPI7	CD.A97
IO3 - GPI8	CD.B85
IO4 - GP05	CD.B91
IO5 - GPO6	CD.B95

Table 4-6 GPIO

PCA955NAME - GPIO NAME	COMX PLUG.PIN
IO6 - GPO7	CD.B101
IO7 - GPO8	CD.B102

4.10 SDHC

The COMX-P40x0 ENP2 module provides an SD/MMC interface to the COM Express connector to support expansion card options on the carrier board.

This module not only supports SD card but also Micro SD card in which there is no write-protect signal. COM Express connector B57 is used to define whether an SD card or Micro SD card is populated on the carrier board.

Table 4-7 SD or Micro SD card on the Carrier

COM Express pin B57	Card on the carrier
1	SD card
0 (Default)	Micro SD card

4.11 SPI Interface

The COMX-P40x0 ENP2 module provides a SPI bus from the P40x0 CPU with 4 chip select signals. All SPI bus signals are routed to COM Express connectors.

4.12 LAN

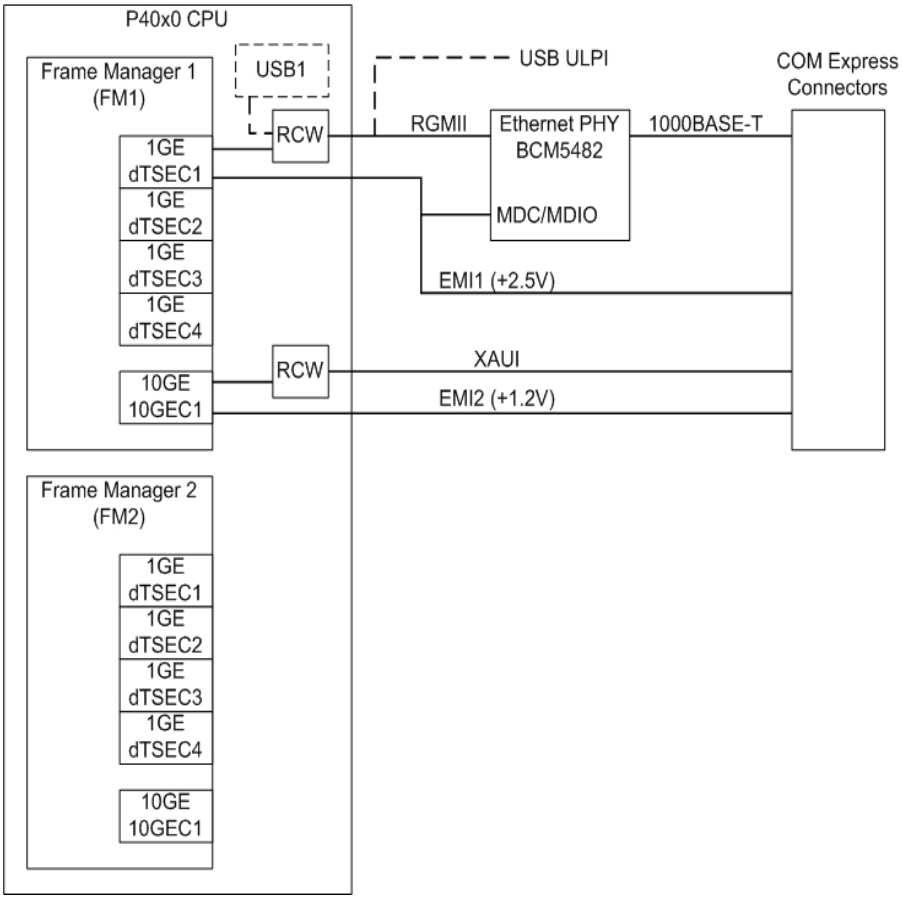
The modules with gigabit Ethernet options route a port with LED control signals to the COM Express connector. The supporting magnetics must be on the carrier board. RGMII is the interface between the P40x0 MAC and external PHY. This interface is multiplexed with the USB1 ULPI interface so modules with the gigabit Ethernet option should set RCW[EC1] to 00 to select RGMII operation.

4.12.1 MDIO

There are two groups of MDIO buses in the P40x0 CPU. The first group called EMI1 complies with IEEE 802.3 Clause 22 and is used for management of the 1Gb Ethernet connection on modules with that option, and management of SerDes interfaces configured as SGMII. EMI1 has two pins: `EMI1_MDC` and `EMI1_MDIO`. All dTSEC interfaces in the P40x0 CPU share the same management hardware. External PHY access for all ports is available through the dTSEC1 registers of FM1. EMI1 is based on +2.5 V signaling levels.

The second group is called EMI2 which complies with IEEE 802.3ae Clause 45 and is used for management of SerDes connections configured for 10GE (XAUI). EMI2 has two pins: `EMI2_MDC and EMI2_MDIO`. External PHY access is performed through the 10GEC registers of FM1. EMI2 is based on +1.2V signaling levels.

Figure 4-7 MDIO Routing



4.13 PHY

The dTSEC1 interface of FM1 is connected to a BCM5482 Ethernet PHY via RGMII on boards with the 1GE option. There are two ports included in the PHY but only the first port is used. The MDIO address for the first port is 0x01 and the second is 0x02.

The MDIO addresses for 4 SGMII PHYs are 0x1C, 0x1D, 0x1E and 0x1F when SerDes option #5/#6 or #10 is applied (or options #7 or #8 when Bank3 is enabled).

4.14 UART Interface

The P40x0 CPU provides up to four UART ports (Tx and Rx signals) or up to two UART ports with hardware flow control (Tx, Rx, RTS, and CTS signals). The COMX-P40x0 ENP2 module is configured by default to route four UART ports to the COM Express connector.

4.15 Real Time Clock

The RTC is implemented by an ST Micro M41T62LC6F device. It is accessed over I2C bus 2 of the P40x0 CPU at address 0xD0. The RTC provides a 32 KHz clock output to the CPU for timekeeping and is supplied by the VCC_BAT pin on the COM Express connector.

4.16 Watchdog Timer

The watchdog timer is implemented by an ST Micro M41T65Q65 device. It is accessed over I2C bus 1 of the P40x0 CPU at address 0xD0. The watchdog timer is capable of generating a power-on reset and interrupt to the CPU.

4.17 USB

The COMX-P40x0 ENP2 module has one USB port from the CPU connected through an USB ULPI PHY (USB3315) to a four-port hub (USB2514). The four ports of the hub are routed to the COM Express connector. The hub is hardware strapped to indicate all ports removable. Two active-low over-current signals are received from the COM Express connector to the USB hub to indicate power faults: USB_OC_0_1_N (Port 0 and 1) and USB_OC_2_3_N (Port 2 and 3).

An optional fifth USB port can be provided from the CPU through a ULPI USB PHY (USB3315) to the COM Express connector. This is the default option for modules not providing the 1GE port since the two functions are multiplexed on the same CPU pins. An active-low over-current signal USB_OC_4_5_N is provided from the COM Express connector to indicate a power fault on the fifth USB port. It is routed as an interrupt to the CPU.

4.18 I2C Interface

The P40x0 CPU has four I2C buses. Among four I2C buses, the I2C bus I2C3 is multiplexed with SDHC bus and remaining I2C buses are routed to the COM Express connectors.

There is only one device attached to the second I2C bus I2C2, and there are 6 devices attached to the first I2C bus I2C1.

The following figure illustrates the distribution of the I2C buses:

Figure 4-8 Distribution of I2C buses

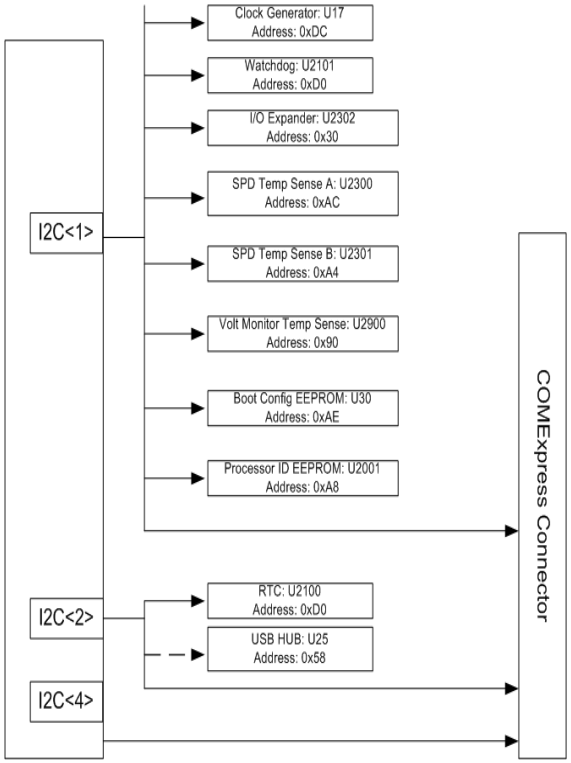


Table 4-8 I2C Interface

Address	Bus	Component	Function
0xDC	I2C1	9FG104DGILFT	Clock Generator
0xD0	I2C1	M41T65Q6F	Watchdog
0x30	I2C1	PCA9557PW-T	IO-Expander
0xAC	I2C1	MCP98243T-BE/ST	SPD Channel A. This is optional and not populated by default.

Table 4-8 I2C Interface

Address	Bus	Component	Function
0xA4	I2C1	MCP98243T-BE/ST	SPD Channel B. This is optional and not populated by default.
0x90	I2C1	ADT7411ARQZ-REEL7	Voltage Monitor/ Temp Sense
0xAE	I2C1	AT24C02-SSHM-T AT24C512C-SSHM-T	2kb Boot Config EEPROM 512kb Boot Config EEPROM
0xA8	I2C1	AT24C512C-XHM-T	Processor ID EEPROM
0xD0	I2C2	M41T62LC6F	RTC
0xDC	I2C2	9FG104DGILFT	Clock Generator

4.18.1 I2C Device Thermal Sensor

The ADT7411 thermal sensor is a dual-channel digital thermometer and under/over temperature alarm. It is located on I2C1 at address 0x90 and measures the CPU temperature.

The ADT7411 can accurately measure the temperature of a remote thermal diode to ±1°C and the ambient temperature to ±3°C. An ALERT output routed to an interrupt on the CPU signals when on-chip or remote temperature is out of range.

4.18.2 I2C Device EEPROM

There are two I2C EEPROMs on the module implemented in AT24C02C and AT24C512C devices. These EEPROMs are located on I2C1; one is for ID EEPROM (U30, AT24C02C, storing board serial number, MAC address and so on.) and the other is for Processor EEPROM (U2001, AT24C512C, storing processor ID and so on).The I2C addresses of these EEPROMs are 0xAE and 0xA8.

The AT24C02C provides 2 Kbits of storage while the AT24C512C provides 512 Kbits.

Both EEPROMs support sequential read and page write.

4.18.3 I2C Device WDT

The watchdog timer M41T65Q is located on I2C1, U2101 and the device address is 0xD0. It is able to generate a power-on reset and interrupt to the CPU.

4.18.4 I2C Device RTC

The real time clock M41T62LC6F is located on I2C2, U2100 and the device address is 0xD0. It provides a 32 KHz clock output and interrupt to the CPU.

4.18.5 I2C Device Clock Generators

One clock generator ICS9FG104 is located on I2C1, U17 and the device address is 0xDC. The second clock generator ICS9FG104 is located on I2C2, U40 with a device address of 0xDC.

The ICS9FG104 is a Frequency Timing Generator that provides four differential output pairs that are compliant to the Intel CK410 specification. The part synthesizes several output frequencies from 25 MHz crystal. It provides outputs with cycle-to-cycle jitter of less than 50 ps and output-to-output skew of less than 35 ps.

Frequency selection can be accomplished via strap pins or SMBus control. By default, strap pins are used.

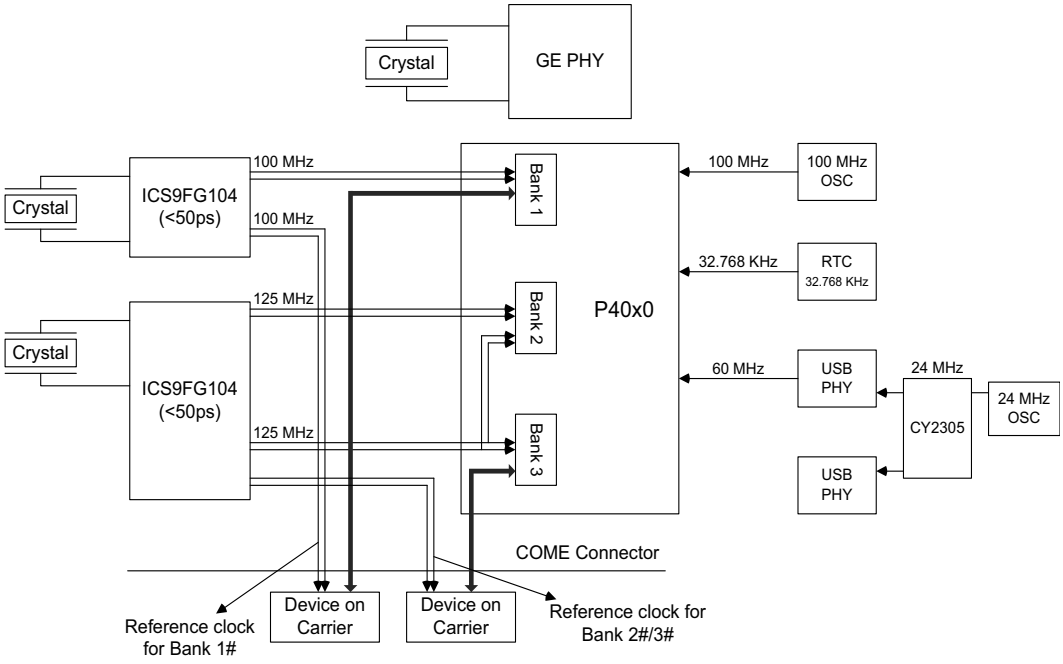
The input clock for the first clock generator is 25 MHz and three differential output pairs are provided. First pair are connected to SerDes Bank 1, second pair are connected to two Aurora connectors, and third pair are connected to COM Express connector. The second clock generator also uses a 25 MHz input reference with three output pairs. The first pair drives SerDes bank 2, the second pair drives SerDes bank 3, and the third is connected to the COM Express connector.

The frequency of the first clock generator (bank 1 SerDes and Aurora) is selected through the FS0 strap pin which is connected to GPIO23 of the CPU and pin B97 of the COM Express connector. The frequency of the second clock generator (bank 2 and 3 SerDes) is also selected through the FS0 strap pin which is connected to GPIO24 of the CPU and pin B98 of the COM Express connector. For first and second clock generators, when FS0 is 0 (low level) the frequency is 100 MHz and when FS0 is 1(high level) the frequency is 125 MHz.

5.1 Overview

The COMX-P40x0 ENP2 module require several kinds of single ended and differential clocks for booting up and normal operation. Following is the clock distribution tree:

Figure 5-1 Clock Distribution



The output frequency of the bank 1 and bank 2/3 SerDes clocks is selectable between 100 MHz and 125 MHz. This must be set correctly by the carrier or corresponding CPU GPIO pins depending on what RCW SerDes configuration is selected. For proper settings, refer *SerDes Block* on page 72.

Table 5-1 Configuration of the frequency of SerDes reference clock by carrier

SerDes bank 1 reference clock select (pin B97 on COM Express)	SerDes bank 2/3 reference clock select (pin B98 on COM Express)
Bank1_SEL_FS0=0, 100 MHz	Bank2_SEL_S1=0, 100 MHz

Table 5-1 Configuration of the frequency of SerDes reference clock by carrier (continued)

SerDes bank 1 reference clock select (pin B97 on COM Express)	SerDes bank 2/3 reference clock select (pin B98 on COM Express)
Bank1_SEL_FS0=1, 125 MHz	Bank2_SEL_S1=1, 125 MHz
*Default:100 MHz	*Default:125MHz

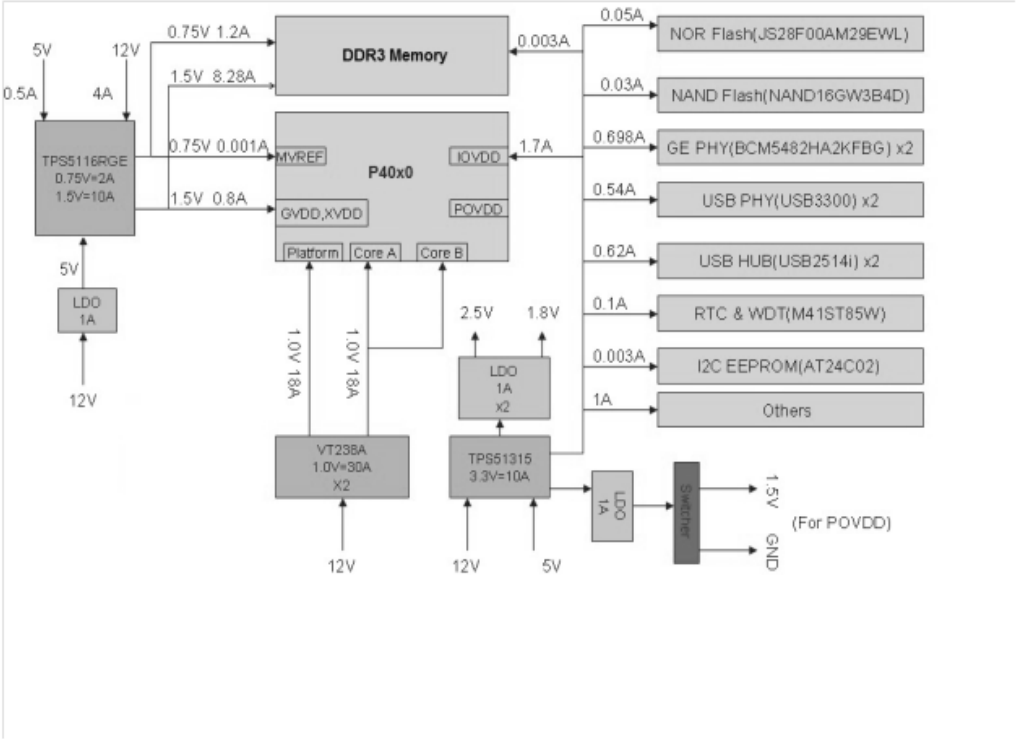
Table 5-2 Configuration of the frequency of SerDes reference clock by GPIO

SerDes bank 1 reference clock	SerDes bank 2 reference clock
CPU_GPIO23=0, 100 MHz	CPU_GPIO24=0, 100 MHz
CPU_GPIO23=1, 125 MHz	CPU_GPIO24=1, 125 MHz
Default:100 MHz	Default:125 MHz

6.1 Overview

This subsection describes the power supply system for the module. 12 V Power is supplied to module from ATX-type (using Artesyn carrier) power supply through COM Express connectors and on-board regulators supply required voltages to devices on the module.

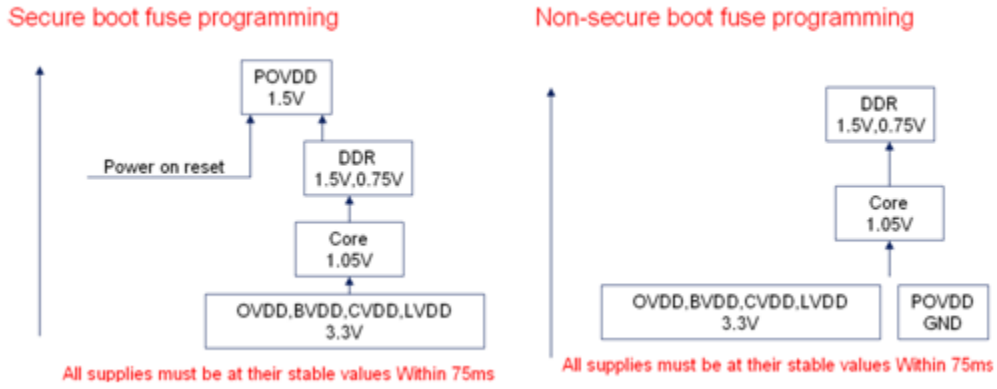
Figure 6-1 Power Tree



6.2 Power Controlling Sequence

The power sequencing of the COMX-P40x0 ENP2 differs between secure boot mode and non-secure boot mode. For secure boot mode, POVDD should be set to 1.5 V DC and is powered at least 100 system clock cycles after the rising edge of power on reset signal. For non-secure boot mode, POVDD should be set to GND.

Figure 6-2 Power Sequence of COMX-P40x0 ENP2



7.1 Overview

The COMX-P40x0-ENP2 module has a Board Support Package (BSP) that provides a shell to allow users to accomplish most of the debugging operations on most of the board's interfaces and peripheral devices. The BSP of the COMX-P40x0 ENP2 module is U-Boot, Linux, DTB and rootfs.

7.2 Setup Requirements

The following are the minimum setup requirements for the COMX-P40x0 ENP2 module:

- One serial cable to connect the COMX-P40x0 ENP2 module to a computer
- One network cable connecting the on-board network port to the network
- A TFTP server connected to the network.
  - The IP address should be192.168.0.100
  - The TFTP root is `/tftpboot/`. You need to create a sub-directory with the name "`comx_p4080/`" in this root.
- Three copies of the BSP package comx_p4080.
- COMX_P4080_V100R00.tar.gz, which will be decompressed in the `comx_p4080/` file
- NFS service is active on this TFTP server and files are exported to `/tftpboot/comx_p4080/rootfs_nfs`

7.3 Basic Commands

The following are the commands commonly used by the U-Boot. To enter the U-Boot shell, press any key while the autoboot is counting down.

Table 7-1 Basic U-Boot Commands

Command	Description
=>	Prompt for the command line.

Table 7-1 Basic U-Boot Commands (continued)

Command	Description
help [cmd] or ? [cmd]	Used to display the usage options for the command "cmd". If "cmd" is not specified, U-Boot will display the brief usage options for all of the available commands.
printenv [vn]	Displays the value of the environment variable "vn". If "vn" is not specified, U-Boot will display the values for all of the environment variables.
setenv <vn> [vv]	Sets the value of the environment variable "vn" to "vv". If "vv" is not specified, U-Boot will not define the environment variable "vn". If "vv" includes spaces, it should be enclosed within single quote marks. For example: `setenv manufacturer 'Emerson Network Power'`
saveenv	Saves all the environment variables persistently to the U-Boot env section on NOR Flash.
run eraenv	Erases all the environment variables stored in the U-Boot env section on NOR Flash. ● Protect off EFEE0000 +00020000; erase EFEE0000 +00020000 ● Protect on EFEE0000 +00020000 A reset must be performed after "run eraenv".
tftpboot	Downloads image through network using TFTP protocol. ● tftpboot [loadAddress] [[hostIPaddr:]bootfilename] ● Example: tftpboot $loadaddr $ubootfile
bootm	Boots application image from memory. ● bootm [addr [arg ...]] ● Example: bootm $norbootaddr $norfsaddr $norfdtaddr ● Example: bootm $loadaddr - $fdtaddr

7.4 BSP Build Requirements

Build Host

The Basic Support Package (BSP) is hosted by an x86 computer running Linux. At least 1 GB free space is required where the BSP is hosted.

Build Tools

Artesyn is using build tools provided in Freescale SDK1.0 QorIQ-DPAA-SDK-20110609-systembuilder.iso to build BSP images.

You can download the Freescale SDK ISO files from and install it on the build host.

7.4.1 Install Build Tools of SDK1.0

Following are the steps to install build tools of SDK1.0 from Freescale SDK on host computer:

1. Login to the Linux host as a non-root user, <user_name>.
2. Copy the `QorIQ-DPAA-SDK-20110609-systembuilder.iso` file to this Linux host.
3. Run the ISO file using the following command:
   ```
   sudo mount -o loop QorIQ-DPAA-SDK-20110609-systembuilder.iso
   /mnt/
   ```
4. Create a `/opt/freescale` directory and update access privileges using the following command:
   ```
   sudo mkdir -p /unixopt/sdk1.0
   sudo chmod a+rwx /unixopt/sdk1.0
   ```
5. Change directory to mount using the following command:
   ```
   cd /mnt/
   ```
6. Install the Freescale LTIB using the following commands:
   ```
   ./install
   <Input /unixopt/sdk1.0 as the installation target directory>
   ```

NOTICE

Do not interrupt the installation process.

7. Execute the `cd /unixopt/sdk1.0/QorIQ-DPAA-SDK-20110609-systembuilder` command.
8. Create a PDK project for P4080DS using the following command:
   `./scripts/create-config.py --config-file=fsl-p4080ds/sample-create-config.ini`
9. Setup cross-compile environment using the `source build_p4080ds_release/bitbake.rc` command.
10. Build Freescale P4080DS BSP images for building test using the `bitbake devel-image` command.

7.5 BSP Source Code Package

7.5.1 De-Compose Source Code Package

Copy the COMX-P4080-2G-ENP2 released BSP source code package `COMX_P4080_SRC_<Version Number>.tar.gz` to the build host and un-compress it in current directory:

```
tar xzvf COMX_P4080_SRC_<Version Number>.tar.gz
```

There will be a newly-created folder named P4080 which contains SCP-P4080-2G-ENP2 source code.

Table 7-2 BSP Source Code Package Layout

File/Directory Name	Description
build.sh	Top script for building all of BSP images for BSP release. It calls Makefile to perform the operations.
clean.sh	Top script for cleaning all of BSP images and temporary objects for BSP release. It calls Makefile to perform the operations.
linux/	linux/ directory contains Linux kernel, rootfs and rootfs building scripts.
Makefile	Top makefile for building/cleaning all of BSP images for BSP release. It calls Makefiles and scripts located in sub-directories to perform the operations.

Table 7-2 BSP Source Code Package Layout

File/Directory Name	Description
Makefile-p4080ds	Top makefile for building/cleaning all of BSP images for P4080DS BSP release. It calls Makefiles and scripts located in sub-directories to perform the operations.
misc/	misc/ contains FMAN uCode and RCW.
u-boot/	U-Boot source code.

7.6 Basic Environment Variable Settings

7.6.1 Setup Build Environment

- If Freescale SDK1.0 is used as build tool, and the host linux is 32-bit, modify the Makefile and set the environment variant PPC_TOOL_PATH as below:

```
SDK_INSTALL_PATH ?= /unixopt/sdk1.0/QorIQ-DPAA-SDK-20110609-
systembuilder
PPC_TOOL_PATH ?= $(SDK_INSTALL_PATH)/freescale-
2010.09/bin:$(SDK_INSTALL_
PATH)/build_p4080ds_release/sysroots/i686-linux/usr/bin
```

NOTICE

The build tool is not verified with SDK1.0 at 64-bit Linux host.

7.6.2 Network Variables

This table lists example network u-boot environment variables to establish a network connection. By default, the factory sets up 10 MAC addresses in the ID EEPROM and u-boot will establish corresponding "ethXaddr" variables automatically.

Network Variables	
setenv ipaddr	192.168.0.91
setenv netmask	255.255.255.0
setenv gatewayip	192.168.0.1
setenv serverip	192.168.0.100

7.6.3 Filename Variables for BSP Components

Filename Variables for BSP Components
setenv rcwfile comx_p4080/COMX_P4080_V100R00/rcw.bin
setenv fmanfile comx_p4080/COMX_P4080_V100R00/fsl_fman_u-code_P4080_101_6.bin
setenv bootfile comx_p4080/COMX_P4080_V100R00/uImage
setenv norfsfile comx_p4080/COMX_P4080_V100R00/rootfs_ext2.img
setenv fdtfile comx_p4080/COMX_P4080_V100R00/comx.dtb
setenv ubootfile comx_p4080/COMX_P4080_V100R00/u-boot.bin
setenv nandfsfile comx_p4080/COMX_P4080_V100R00/rootfs_jffs2.nand
setenv rootpath /tftpboot/comx_p4080/rootfs_nfs

7.6.4 Address Variables for BSP Components on NOR Flash

Address Variables for BSP Components on NOR Flash	
norrcwaddr	Default is E8000000
norfmanaddr	Default is E8200000
norfsaddr	Default is E9000000
norbootaddr	Default is EE000000
norfdtaddr	Default is EFD00000
norubootenvaddr	Default is EFEE0000
norubootaddr	Default is EFF00000

7.6.5 Address Variables for the Boot Components in RAM

Address Variables for the Boot Components in RAM	
loadaddr	Default is 1000000
fdtaddr	Default is C0000
ramdiskaddr	Default is 2000000

7.6.6 Device Variables

Device Variables
setenv ethact FM1@DTSEC1
setenv netdev eth0
setenv uart# 0
setenv consoledev ttyS0

setenv baudrate 115200
setenv usbbdev sda2
setenv mmcbdev mmcblk0p2
setenv hdbdev sda1
setenv jffs2nand mtdblock7

7.6.7 HWCONFIG Variable

HWCONFIG Variable	
hwconfig	Default is ‘fsl_ddr:ctlr_intlv=cache-line,bank_intlv=cs0_cs1;esdhc;SerDes:fsl_srds_lp-d_b3=0xf;fsl_fm2_xaui_phy:xfi’.

7.6.8 Bootargs Variable

Bootargs Variable	
root	• root=/dev/ram for ramboot and norboot; • 'root=/dev/$jffs2nand rw’ for nandboot; • root=/dev/nfs for nfsboot; • 'root=/dev/$usbbdev rw’ for usbfatboot and usbext2boot; • oot=/dev/$mmcbdev rw’ for mmcfatboot and mmcext2boot
rootfstype	‘rootfstype=jffs2’ is needed for nandboot
rootdelay	‘rootdelay=30’ is needed for usb*boot and mmc*boot
console	Default is ‘console=$consoledev,$baudrate’
hwbootargs	Default is ‘riohdid=0 xauiphy=1’, generated by U-Boot based on hwcon-fig.
othbootargs	Default is ‘ramdisk_size=00700000 cache-sram-size=0x10000

7.6.9 Bootup Variables

Bootup Variables	
ramboot	Default is 'setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate $hwbootargs $othbootargs;tftp $ramdiskaddr $ramdiskfile;tftp $loadaddr $bootfile;tftp $fdtaddr $fdtfile;bootm $loadaddr $ramdiskaddr $fdtaddr'
norboot	Default is 'setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate $hwbootargs $othbootargs;bootm $norbootaddr $norfsaddr $norfdtaddr'
nandboot	Default is 'setenv bootargs root=/dev/$jffs2nand rw console=$consoledev,$baudrate rootfstype=jffs2 $hwbootargs $othbootargs;bootm $norbootaddr - $norfdtaddr'
nfsboot	Default is 'setenv bootargs root=/dev/nfs rw nfsroot=$serverip:$rootpath ip=$ipaddr:$serverip:$gatewayip:$netmask:$hostname:$netdev:off
mmcfatboot	default is 'setenv bootargs root=/dev/$mmcbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;mmcinfo;fatload mmc 0:1 $loadaddr /boot/$bootfile;fatload mmc 0:1 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'
mmcext2boot	default is 'setenv bootargs root=/dev/$mmcbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;mmcinfo;ext2load mmc 0:2 $loadaddr /boot/$bootfile;ext2load mmc 0:2 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'
usbfatboot	default is 'setenv bootargs root=/dev/$usbbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;usb start;fatload usb 0:1 $loadaddr /boot/$bootfile;fatload usb 0:1 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'
usbext2boot	default is 'setenv bootargs root=/dev/$usbbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;usb start;ext2load usb 0:2 $loadaddr /boot/$bootfile;ext2load usb 0:2 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'

7.7 Checking the BSP Version

There are several different versions of the BSP, but no versions are available for RCW and DTB. Below are the methods followed to check versions of the BSP.

1. For the FMAN uCode Version, it is found in the U-Boot boot-up message.
   Fman: Uploading microcode version 101.6.0.

2. RAMDISK rootfs version

   - Boot up with ramboot ('run ramboot' in U-Boot) or norboot ('run norboot' in U-Boot).
     In Linux, run `'cat /etc/.version'`

```
[root@COMX-P4080 root]# cat /etc/.version
COMX-P4080 EXT2 ROOTFS ver: COMX_P4080_V100R00 build by
ec7536@cncdebaobs04.emrsn.org on Mon Nov 29 08:46:50 UTC 2010
```

3. Kernel version

   - The version is viewed in the loading kernel message:
     ## Booting kernel from Legacy Image at XXXXXXXX ...
     Image Name: Linux-2.6.34.6
     Created: 2010-11-29 8:46:16 UTC

   - Run 'iminfo $norbootaddr' in U-Boot

```
=> iminfo $norbootaddr
## Checking Image at ee000000 ...
Legacy image found
Image Name:   Linux-2.6.34.6
Created:      2010-11-29   8:46:16 UTC
Image Type:   PowerPC Linux Kernel Image (gzip compressed)
Data Size:    3520445 Bytes = 3.4 MiB
Load Address: 00000000
Entry Point:  00000000
Verifying Checksum ... OK
```

   - In the kernel boot-up message:

```
Linux version 2.6.34.6 (ec7536@cncdebaobs04.emrsn.org) (gcc
version 4.3.2 (Sourcery G++ Lite 4.3-74) ) #1 SMP Mon Nov 29
16:46:03 CST 2010
```

4. U-Boot Version

   - Run the command "version" after the first line of the U-Boot boot-up message

     ```
     => version
     U-Boot 2010.06-COMX_P4080_V100R00 (Nov 29 2010 - 16:24:12)
     ```

5. JFFS2 rootfs version

   - In the U-Boot, boot with nandboot ('run nandboot'). In Linux, run '`cat /etc/.version`'

     ```
     [root@COMX-P4080 root]# cat /etc/.version
     COMX-P4080 JFFS2 ROOTFS for nand.full FLASH ver:
     COMX_P4080_V100R00 build by ec7536@cncdebaobs04.emrsn.org on
     Mon Nov 29 08:47:50 UTC 2010
     ```

6. NFS rootfs version

   - In the U-Boot, boot with nfs ('run nfsboot'). In Linux, run '`cat/etc/.version`'.

     ```
     [root@COMX-P4080 root]# cat /etc/.version
     COMX-P4080 NFS ROOTFS ver: COMX_P4080_V100R00 build by
     ec7536@cncdebaobs04.emrsn.org on Mon Nov 29 08:50:20 UTC 2010
     ```

7.8 CPU

The COMX-P4080 module has the Freescale QorIQ Communications Processor. The CPU information can be viewed in the terminal. Figure 7-1 below shows console output containing an example of the CPU information.

Figure 7-1 COMX-P4080 CPU Information

```
U-Boot 2010.06-COMX_P4080_V100R00 (Nov 29 2010 - 16:24:12)

CPU0:  P4080E, Version: 2.0, (0x82080020)
Core:  E500MC, Version: 2.0, (0x80230020)
Clock Configuration:
       CPU0:1500 MHz, CPU1:1500 MHz, CPU2:1500 MHz, CPU3:1500 MHz,
       CPU4:1500 MHz, CPU5:1500 MHz, CPU6:1500 MHz, CPU7:1500 MHz,
       CCB:800  MHz,
       DDR:650  MHz (1300 MT/s data rate) (Asynchronous), LBC:25   MHz
       FMAN1: 600 MHz
       FMAN2: 600 MHz
       PME:   400 MHz
L1:    D-cache 32 kB enabled
       I-cache 32 kB enabled
```

CPU0 is the active CPU in the U-Boot. Run the command "`reset`" to reboot the CPU/board.

7.9 Address Space

U-Boot and Linux works in 36-bit physical addressing mode. The relationship between effective address and physical address is displayed in the memory map table on Table "COMX-P4080 Address Space".

The following are mapped in to the first 4 GB address space of the 64 GB, which is the 36-bit physical address space. The 4 GB space is named as the effective address space and is accessed by the U-Boot.

- DDR3 SDRAM
- PCIE1/2/3 MEM
- PCIE1/2/3 IO
- RIO1/2 MEM
- LBC NOR FLASH
- DCSR
- BMAN MEM
- QMAN MEM
- NAND FLASH Buffer
- CCSR
- BOOT PAGE

Table 7-3 COMX-P4080 Address Space

Address	32-bit Effective Base Address	36-bit Physical Base Address	Size	Description
1	0000 0000	0 0000 0000	8000 0000 - 2 GB	DDR3 Memory
2	8000 0000	C 0000 0000	2000 0000 - 512 MB	PCIE1 MEM
3	A000 0000	C 2000 0000	2000 0000 - 512 MB	PCIE2 MEM, if #4 and #5 are unused
4	A000 0000	C 2000 0000	1000 0000 - 256 MB	RIO1 MEM, if #2 is unused

Table 7-3 COMX-P4080 Address Space (continued)

Address	32-bit Effective Base Address	36-bit Physical Base Address	Size	Description
5	B000 0000	C 3000 0000	1000 0000 - 256 MB	RIO2 MEM, if #2 is unused
6	C000 0000	C 4000 0000	0800 0000 - 512 MB	PCIE3 MEM
7	E800 0000	F E800 0000	0800 0000 - 128 MB	LBC NOR Flash
8	F000 0000	F 0000 0000	0040 0000 - 4 MB	DCSR
9	F400 0000	F F400 0000	0020 0000 - 2 MB	BMAN MEM
10	F420 0000	F F420 0000	0020 0000 - 2 MB	QMAN MEM
11	F800 0000	F F800 0000	0001 0000 - 64 KB	PCIE1 IO
12	F801 0000	F F801 0000	0001 0000 - 64 KB	PCIE2 IO
13	F802 0000	F F802 0000	0001 0000 - 64 KB	PCIE3 IO
14	FFA0 0000	F FFA0 0000	0010 0000 - 1 MB	NAND Flash Buffer
15	FE00 0000	F FE00 0000	0100 0000 - 16 MB	CCSR
16	FFFF F000	0 FFFF F000	0000 1000 - 4 KB	Boot Page

U-Boot uses the following commands to display and modify the contents of the 4 GB effective address space. Note that ".b", ".w", and ".l" means the operation unit as "byte", "word", and "long" respectively.

md - Memory display
md [.b, .w, .l] address [# of objects]

mm - memory modify (auto-incrementing address)
mm [.b, .w, .l] address

nm - memory modify (constant address)
nm [.b, .w, .l] address

cp - this command copies data from one place to another
cp [.b, .w, .l] source target count

cmp - this command compares two data in different places.
cmp [.b, .w, .l] addr1 addr 2 count

7.10 DDR3 SDRAM

The COMX-P4080 module has two fully programmable DDR3 SDRAM controllers. A maximum of 2 GB SDRAM are mapped in U-Boot. If more than 2 GB SDRAM is fitted, the remaining sections are left unmapped. With Linux, up to 4 GB SDRAM can be verified.

Do not modify the contents of the lowest 1 MB and the top 1 MB RAM in the U-Boot. Both areas are used to store critical data by U-Boot.

When the U-Boot detects the DDR3 SDRAM during boot up, the following message appears:

```
DRAM: Initializing...
2 GB left unmapped
    DDR: 4 GB (DDR3, 64-bit, CL=9, ECC on)
    DDR Controller Interleaving Mode: cache line
    DDR Chip-Select Interleaving Mode: CS0+CS1
```

7.11 GPIO

The COMX-P40x0-ENP2 module has 20 general purpose input/output (GPIO), 12 connected to the CPU, and 8 implemented on an I2C expander. For more information, see *GPIO* on page 78.

Table 7-4 GPIO States

GPIO#	Input/Output	Reset State	Description
GPIO00	I	I	GPI0 of COM-E connectors
GPIO01	I	I	GPI1 of COM-E connectors
GPIO02	I	I	GPI3 of COM-E connectors
GPIO03	I	I	GPI4 of COM-E connectors
GPIO04	O	I	GPO0 of COM-E connectors and also as to control debug LED D18
GPIO05	O	I	GPO1 of COM-E connectors and also as to control debug LED D19
GPIO06	O	I	GPO3 of COM-E connectors

Table 7-4 GPIO States (continued)

GPIO#	Input/Output	Reset State	Description
GPIO07	O	I	GPO4 of COM-E connectors
GPIO19	O	I	Clock Generator Enable
GPIO20	O	I	Carried board reset output
GPIO23	I	I	Clock generator of bank 1 frequency selection input
GPIO24	I	I	Clock generator of bank 2/3 frequency selection input

For more information, see *GPIO* on page 78.

The U-Boot provides several GPIO utility commands.

Table 7-5 GPIO Command Usage

Command	Description
gpio dump	Dumps the direction, od and level information for all pins
gpio get <pin>	Gets the direction, od and level information for the specified pin
gpio set dir <pin> <dir>	Sets the direction of the specified pin
gpio set dir <pin> <od>	Sets the od of the specified pin
gpio set dir <pin> <lvl>	Sets the level of the specified pin

The parameters used in the GPIO utility commands are described below.

<pin> - 0, 1, 2, 3, 4, 5, 6, 7, 19, 20, 23, 24

<dir> - 0 for input
1 for output

<od> - 0 for output
1 for open drain

<lvl> - 0 for low level
1 for high level

For the GPIO signals connected to the I2C expander, these are controlled via the "i2c" command using the I2C address = 0x18. For more information, see *I2C* on page 110.

7.12 UART

There are four universal asynchronous receiver/transmitters (UART) in the COMX-P40x0 ENP2 module, each with Tx and Rx signals routed to the COM-E connectors.

The default active console is UART0. The working mode is 115200baud rate, 8 data bit, No parity, 1 stop bit. Each of the four UART can become the active console by setting the environment variable "uart#".

Usage:

UART0 - setenv uart# 0; saveenv; reset

UART1 - setenv uart# 1; saveenv; reset

UART2 - setenv uart# 2; saveenv; reset

UART3 - setenv uart# 3; saveenv; reset

The UART boot up message in U-Boot is as follows:

```
In :                Serial
Out :               Serial
Err :               Serial
Current Console:    uart#0
```

7.13 NOR Flash

The NOR Flash is Numonyx™ Axcell™ JS28F00AM29EWL or Spansion S29GL01GP11TFIR2 and is attached to the GPCM on local bus and works with 16-bit data width. It is either 1 GB or 128 MB and has 1024 uniform blocks of 128 K (or 64 K words each). The 36-bit physical address of NOR Flash is 0xFE8000000 - 0xFEFFFFFFF. Boot up message in U-Boot is "FLASH: 128 MiB".

NOR Flash supports the following commands: md, cp, cmp, protect and erase.

Table 7-6 NOR Flash Command Usage

Command	Description
protect on start end	Protects flash from address "start" to address "end"
protect on start +len	Protects flash from address "start" to end of section with address "start"+"len"-1
protect on all	Protects all flash banks
protect off start end	Makes flash from address "start" to address "end" writable
protect off start +len	Makes flash from address "start" to end of section with address "start"+"len"-1 writable
protect off all	Makes all flash banks writable
erase start end	Erases flash from address 'start' to address 'end'
erase start +len	Erases flash from address 'start' to the end of section with address 'start'+len-1
erase all	Erases all flash banks

The following is a NOR Flash operation example that upgrades the U-Boot.

```
tftpboot $loadaddr $ubootfile; protect off 0xeff00000 +$filesize;
erase 0xeff00000 +$filesize; cp.b $loadaddr 0xeff00000 $filesize;
protect on 0xeff00000 +$filesize;
```

7.14 NAND Flash

The NAND Flash is Numonyx NAND08GW3B2CN6E which is 1 GB in size. It is attached to the FCM on the local bus and works at 8-bit mode. Boot up message will appear as "NAND: 1024 MiB".

Each page contains 2,112 bytes, including 2048 bytes of data with 64 bytes spare. Each block contains 64 pages, including 128 KB of data with 4 KB spare, making a total of 8192 blocks.

NAND Flash supports the following commands:

Table 7-7 NAND Flash Command Usage

Command	Description
nand info	Shows available NAND devices
nand device [dev]	Shows or sets current device
nand read	Addr off | partition size
nand write	Addr off | partition size Read/write 'size' bytes starting at offset 'off' to/from memory address 'addr', skipping bad blocks.
nand erase [clean] [off size]	Erase 'size' bytes from offset 'off' (will erase on the entire device if it is not specified)
nand bad	Shows bad blocks
nand dump[.oob] off	Dumps page
nand scrub	Cleans NAND by erasing bad blocks. Considered unsafe.
nand markbad off [...]	Marks bad block or blocks at offset. Considered unsafe.
nand biterr off	Makes a bit error at offset. Considered unsafe.

7.15 I2C

There are four I2C buses in the COMX-P40x0 ENP2 module, labeled as I2C<1/2/3/4>. For more information, see *GPIO* on page 78.

U-Boot provides the following utilities for I2C bus and devices.

Table 7-8 U-Boot I2C Utilities

Utility	Description
i2c crc32 chip address[.0, .1, .2] count	Compute CRC32 checksum
i2c dev [dev]	Shows or sets current I2C bus
i2c loop chip address[.0, .1, .2] [# of objects] [# of delay(us)]	Loops reading of device
i2c md chip address[.0, .1, .2] [# of objects]	Reads from I2C device
i2c mm chip address[.0, .1, .2]	Writes to I2C device (auto-incrementing)
i2c mw chip address[.0, .1, .2] value [count]	Writes to I2C device (fill)
i2c nm chip address[.0, .1, .2]	Writes to I2C device (constant address)
i2c probe	Shows devices on the I2C bus
i2c read chip address[.0, .1, .2] length memaddress	Reads to memory
i2c reset	Re-initializes the I2C Controller
i2c speed [speed]	Shows or set I2C bus speed

I2C buses in the U-Boot have been re-assigned as follows:

'i2c dev 0' selects I2C<1>

'i2c dev 1' selects I2C<2>

'i2c dev 2' selects I2C<4>

The devices displayed via the "i2c probe" command are 7-bit I2C addresses. The addresses found in the HW Table 4-8 on page 86 are 8-bit addresses. (For example: 7-bit address 0x18 corresponds to the 8-bit address 0x30)

7.15.1 ID EEPROM

An I2C EEPROM AT24C02 (U30) is used as the ID EEPROM, located on I2C<1>. The COMX-P40x0 ENP2 module uses ID EEPROM to store the board's serial number, number of network ports, MAC addresses, errata level, manufacturing date and other information. Boot up message in the U-Boot will be: "EEPROM: NXID v0".

U-Boot provides several "mac" utilities to display and program the data in ID EEPROM.

```
mac [read|save|id|num|errata|date|ports|0|1|2|3|4|5|6|7]
```

mac read	Shows content of EEPROM
mac save	Saves to the EEPROM
mac id	Programs system id
mac num	Programs system serial number
mac errata	Programs errata data
mac date	Programs date
mac ports	Programs the number of ports
mac X	Programs the MAC address for port X [X=0...7]

The following are usage examples:

- mac id
- mac num E017D99
- mac errata 0
- mac date 101021120000
- mac ports 1
- mac 0 00:80:42:05:49:d4
- mac save

7.15.2 Board EEPROM

An I2C EEPROM AT24C512 (U2001) is used as the BOARD EEPROM, located on I2C<1>. The COMX-P40x0 ENP2 module uses BOARD EEPROM to store information about the board's processor family, module family and configuration, among others. Boot up message in U-Boot will appear as "EEPROM: COMX".

The U-Boot provides "brd" utilities to display and program the data in BOARD EEPROM.

```
brd [read|save|id|pf|pv|pe|mf|mv|me|ms|md|ma]
```

read	Shows content of EEPROM
brdsave	Saves to the EEPROM
brd id	Programs board id
brd pf	Programs processor family
brd pv	Programs processor version
brd pe	Programs processor errata
brd mf	Programs module family
brd mv	Programs module version
brd me	Programs module errata
brd md	Programs module description string
brd ms	Programs memory size
brd ma	Programs manufacturer string

The following are usage examples of "brd" on the COMX-P40x0 ENP2 module.

- brd id
- brd pf P4080
- brd pv B
- brd pe 00
- brd mf COME1
- brd mv GA

- brd me 00
- brd ms 4096
- brd md 'ComExpress module on P4080(1.5GHz)'
- brd ma 'Emerson Network Power'
- brd save

7.15.3 Real Time Clock (RTC) and Watchdog Timer (WDT)

The COMX-P40x0 ENP2 module uses RTC and Watchdog features on M41ST85W. The I2C RTC/WDT M41ST85W (U12) is adopted on the COMX-P40x0 ENP2 and located on I2C<1>.

Boot up message in the U-Boot will be as follows: "RCT: M41ST85W@68" and "WDT: M41ST85W@68(disabled)".

U-Boot provides "date" commands to operate the RTC features. These include get/set/reset date and time.

```
date [MMDDhhmm[[CC]YY][.ss]]
```

date reset

without arguments:	Prints date and time
with numeric argument:	Sets the system date and time
with 'reset' argument:	Resets the RTC

The following are usage samples for "date" on the COMX-P40x0 ENP2.

- date
  Date: 2010-12-01 (Wednesday) Time: 17:57:37
- date reset
  Reset RTC
  Date: 2010-18-01 (Sunday) Time: 0:00:00
- date 120117592010.00
  Date: 2010-12-01 (Wednesday) Time: 17:59:00

U-Boot provides "wdt" commands to operate on the WDT features.

wdt reset	-	Resets WDT
wdt status	-	Checks the current status of WDT
wdt disable	-	Disables WDT
wdt enable <timeout#>	-	Enables WDT with timeout <timeout#> seconds. <timeout#> range [1...124]

The following are usage examples of "wdt" for the COMX-P40x0 ENP2 module.

- wdt status
  WDT: disabled.
- wdt enable 5
  WDT: enabled with timeout 5 seconds.
- wdt reset
  System reset.

7.15.4 DTT

An I2C thermal sensor ADT7411 (U36) is installed and is located on I2C<1>. The ADT7411 is used to monitor the CPU temperature. Boot up message in the U-Boot will read as "DTT: ADT7411@4C".

U-Boot provides "dtt" to display the CPU temperature. Here is an example of dtt usage:

- dtt
  DTT1: CPU Temperature: 48 C

7.16 SPI

The COMX-P40x0 ENP2 module provides a SPI bus from the P40x0 CPU with four chip-select signals. All SPI bus signals are routed to COM Express connectors.

For more information on the distribution of the SPI bus, see *SPI Interface* on page 81.

U-Boot provides "sf" utilities to operate SPI Flash.

sf probe [bus:]cs [hz] [mode]	-	Initializes flash device on given SPI bus and chip select.
sf read addr offset len	-	Reads 'len' bytes starting at 'offset' to memory at 'addr'
sf write addr offset len	-	Writes 'len' bytes from memory at 'addr' to flash at 'offset'
sf erase offset len	-	Erases 'len' bytes from 'offset'

Below are usage samples for "sf".

- sf probe 0
  4096 KiB S25FL032A(P) at 0:0 is now current device
- sf erase 0 80000
- sf read 1000000 0 10000
- sf write 1000000 0 10000

7.17 MMC/SDHC

The COMX-P40x0 ENP2 module provides a MMC/SDHC interface to the COM Express connector. There is also a connector for this provided on the carrier. By default, the MMC/SDHC 4-bit mode is selected.

U-Boot provides "mmcinfo" and "mmc" utilities to operate the MMC/SDHC card. "mmcinfo" must be executed before other "mmc" commands can be run.

mmcinfo		
mmcread <device num> addr blk# cnt		
mmc write <device num> addr blk# cnt		
mmc rescan <device num>		
mmc list	-	Lists available devices

7.18 USB

The COMX-P40x0 ENP2 module has four USB ports. For more information on the *USB* on page 84.

U-Boot provides "usb" utilities to operate the USB sticks:

Utility	Function
usb reset	Resets or rescans USB controller
usb stop [f]	Stops USB [f]=force stop
usb tree	Shows USB device tree
usb info [dev]	Shows available USB devices
usb storage	Shows details of USB storage devices
usb dev [dev]	Shows or set current USB storage device
usb part [dev]	Prints partition table of one or all USB storage devices
usb read addr blk# cnt	Reads `cnt' blocks starting at block `blk#' to memory address `addr‘
usb write addr blk# cnt	Writes `cnt' blocks starting at block `blk#' from memory address `addr'

Note that "usb start/reset" must be executed before the other commands can be run. Below are usage samples of "usb start.

```
=> usb start
(Re)start USB...
USB: Register 10011 NbrPorts 1
USB EHCI 1.00
scanning bus for devices... 3 USB Device(s) found
scanning bus for storage devices... 1 Storage Device(s) found
```

7.19 SerDes

The COMX-P40x0 ENP2 module has three Serializer/Deserializer (SerDes) banks, including a total of 18 lanes.

For more information on the SerDes, see *SerDes Block* on page 72. This includes the SerDes lane distribution and options when it is routed to the COM Express connectors.

U-Boot provides "rcw" utilities to switch SerDes lanes among the twelve SerDes/RCW options. A checking feature is also supported. Below is a usage sample of the utilities.

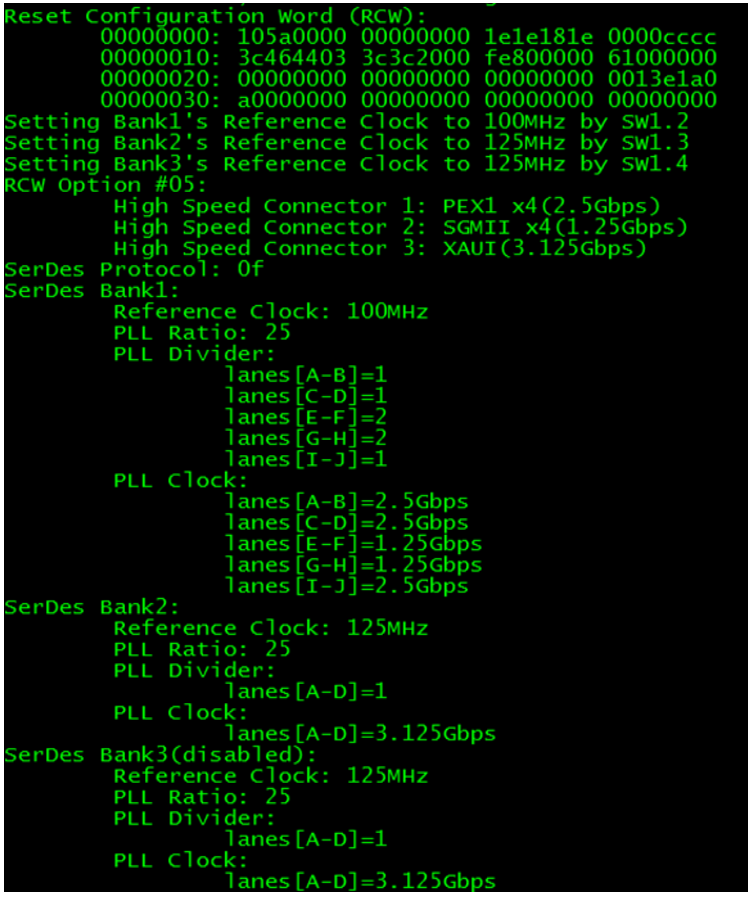
rcw list	-	Lists the status of RCW sections
rcw active <option#>	-	active <option#> RCW. <option#> range [1..12]
rcw check current	-	Checks the current RCW with which system boots up
rcw check active	-	Checks the status of the active RCW section
rcw check backup [option#]	-	Checks the status of all or # backup RCW section(s). <option#> range [1..12]

The steps below are used to activate specific SerDes/RCW options.

- Run "rcw active <option#>" to activate the SerDes/RCW option#.
- Power off the board.
- For RCW options #7 or #8, a means to change the SerDes clock settings must be provided by the customer's carrier board.
- Power up the board.

Using option #5 from Table "Options of the SerDes routed to COM Express Connectors" on page 73 as an example, the boot up message will appear as below.

Figure 7-2 Example of Boot Up Message in U-Boot



7.20 Network

The COMX-P40x0 ENP2 module has two frame managers. Each one supports five native network interfaces broken down into four 1 GB Ethernet interfaces (DTSEC) and one 10 GB Ethernet interface (TGEC). Due to limitations in the CPU and frame manager, only 12 Gbps is supported. This does not allow the DTSEC and one XAUI to work the line speed at the same time at 14 Gbps.

Because of these limitations, the COMX-P40x0-ENP2 powers down the XAUI interface for RCW options #5 and #6. The total line speed must not exceed 12Gbps for these configurations.

The COMX-P40x0 ENP2 has the following combinations of network ports in the frame managers:

- 1 RGMII (FM1) + XAUI (FM2) RCW options: 1-4, 9, 11-12
- 1 RGMII (FM1) + 4 SGMII (FM2) RCW options: 5-6
- 1 RGMII (FM1) only (+ SRIO configuration) RCW options 7-8

PCI Express based network ports like the Intel PRO/1000 are not limited by the above mentioned rules because their packets are handled not by the frame managers but by the CPU. The COMX-P40x0 ENP2 powers down the Bank 3 SerDes (FM1 lanes).

EC1 of pin multiplexing configuration in the RCW routes the RGMII port (FM1@DTSEC1) to the EC1 parallel mode pins. The RGMII port is always present in all of the twelve SerDes/RCW options.

Table 7-9 Network Ports Naming Rules in U-Boot

FM1 Network Ports	
	Port 0 (the RGMII port) is named as FM1@DTSEC1
FM2 Network Ports	
	Port 0 is named as FM2@DTSEC1
	Port 1 is named as FM2@DTSEC2
	Port 2 is named as FM2@DTSEC3
	Port 3 is named as FM2@DTSEC4
	Port 4 (XAUI) is named as FM2@TGEC1

With one SGMII-Riser (Freescale), one XAUI-Rise (Freescale), two PRO/1000 Server Adapter (Intel), the valid combinations of network ports among the twelve SerDes/RCW options are listed in Table "Valid Network Ports Combination of SerDes/RCW" on page 121.

Refer to Table "Options of the SerDes routed to COM Express Connectors" on page 73 for the corresponding information on SerDes 0-3, SerDes 4-7 and SerDes 10-13 for each option.

Table 7-10 Valid Network Ports Combination of SerDes/RCW

Option	Onboard RGMII	SGMII-Riser	XAUI-Riser	PRO/1000 (dual-port) #1	PRO/1000 (dual-port) #2
1	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
2	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
3	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
4	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
5	FM1@DTSEC1	SLOT J14 FM2@DTSEC1 FM2@DTSEC2 FM2@DTSEC3 FM2@DTSEC4	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X
6	FM1@DTSEC1	SLOT J14 FM2@DTSEC1 FM2@DTSEC2 FM2@DTSEC3 FM2@DTSEC4	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X
7	FM1@DTSEC1	X	X	SLOT J6 e1000#0 e1000#1	X

Table 7-10 Valid Network Ports Combination of SerDes/RCW (continued)

Option	Onboard RGMII	SGMII-Riser	XAUI-Riser	PRO/1000 (dual-port) #1	PRO/1000 (dual-port) #2
8	FM1@DTSEC1	X	X	SLOT J6 e1000#0 e1000#1	X
9	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	X	X
10	FM1@DTSEC1	SLOT J10 FM2@DTSEC1 FM2@DTSEC2 FM2@DTSEC3 FM2@DTSEC4	X	X	X
11	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X
12	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X

During Linux boot up, every network port is named "ethX" by default. UDEV rules, allow it to be changed by the user.

The "x" in the name is important for the nfsboot. For more information, see Chapter 7, *Boot, on page 129*. To locate the X "x" in the "ethX", refer to the list below.

0 - FM2@DTSEC1

1 - FM2@DTSEC1

2 - FM2@DTSEC2

3 - FM2@DTSEC3

4 - FM2@DTSEC4

5 - FM2@TGEC1

6 - e1000#0

7 - e1000#1

8 - e1000#2

9 - e1000#3

If certain frame manager network port or ports are not valid for the specified SerDes/RCW option, the “X” for the lower valid network port should subtract the numbers of the above invalid network ports.

Here is an example of the "ethX" naming based on the option #5. Install Intel PRO/1000 server adapter in SLOT J6. For the Freescale SGMII-Riser install it in SLOT J14 and for Freescale XAUI-Riser, install it in SLOT J10. The U-Boot boot up message will list the valid ports list: FM1@DTSEC1,FM2@DTSEC1,FM2@DTSEC2,FM2@TGEC1, e1000#0, e1000#1. The "ethX" list would then be as follows:

0 - FM1@DTSEC1

1 - FM2@DTSEC1

2 - FM2@DTSEC2

* - FM2@DTSEC3

* - FM2@DTSEC4

3 (5-2) - FM2@TGEC1

4 (6-2) - e1000#0

5 (7-2) - e1000#1

* - e1000#2

* - e1000#3

UDEV rules, rename the default name "ethX" for network ports of frame manager for convenience and identification.

Table 7-11 UDEV Rules for Network Ports in Linux

FM1 Network Ports
Port 0 (FM1@DTSEC1) is named as fm1-gb1

Table 7-11 UDEV Rules for Network Ports in Linux (continued)

FM1 Network Ports
FM2 Network Ports
Port 0 (FM2@DTSEC1) is named as fm2-gb1
Port 1 (FM2@DTSEC2) is named as fm2-gb2
Port 2 (FM2@DTSEC3) is named as fm2-gb3
Port 3 (FM2@DTSEC4) is named as fm2-gb4
Port 4 (FM2@TGEC1) (XAUI) is named as fm2-10g

An exception for frame manager network ports is when the nfsboot, which is the network port for mounting NFS, remains "ethX" and will not be renamed to "fmY-gbZ" in Linux because the udev cannot rename the device that is currently busy.

For network ports of PRO/1000, the port name is always "ethX".

7.21 Build BSP Images

Output Directory

By default, the output directory for building BSP images is `/local/tmp/`.You need to create this directory and provide full privileges for all users to access. Use the following commands to create directory and provide privileges:

```
sudo mkdir -p
```

```
sudo chmod a+rwx /local/ /local/tmp/
```

Build a Release

To build a release, run the `./build.sh <Version_Number>` command.

NOTICE

The version number is formatted as VxxxAxx, VxxxBxx, VxxxTxx or VxxxRxx. For example: V100B00.

BSP Images

SCP-P4080-2G-ENP2 BSP images should be placed in `/local/tmp/`. It includes the `COMX_P4080_<Version_Number>.tar.gz` package:

The `COMX_P4080_<Version_Number>.tar.gz` package contains:

- `comx.dtb`: Device Tree Blob
- `fsl_fman_ucode_P3_P4_P5_101_8.bin`: FMAN uCode
- `rcw.bin`: RCW
- `rcw-codewarrior.bin`: RCW used for code warrior to burn image to NOR Flash
- `rootfs_ext2.img`: RAMDISK image
- `rootfs_nfs.tar.gz`: NFS rootfs
- `u-boot.bin` (U-Boot)
- `uImage`: Linux kernel image

7.21.1 Build U-Boot

The U-Boot is based on SDK1.0 whose version is `U-Boot 2011.06-rc2`.

Commands

1. Build by default
   - `make uboot`
2. Build Targets supported for U-Boot
   - `uboot`: configures and builds `u-boot.bin` for NOR flash
   - `uboot-clean`: cleans the U-Boot

Output

The built image is `u-boot.bin` in the current working directory.

7.21.2 Build Linux Kernel

The Linux kernel is based on SDK1.0 whose version is 2.6.34.6.

Commands

1. Build by default
   - `make kernel dtb`
2. Build Targets supported for Linux kernel
   - `config-default`: copies the COMX-P4080 default configuration to current configuration
   - `kernel-config`: configures the kernel based on current configuration
   - `kernel`: compiles kernel with current configuration
   - `kernel-clean`: cleans the kernel
   - `dtb`: compiles device tree binary

Output

The build images are `uImage` and `comx.dtb` in the current working directory.

7.21.3 Build ROOTFS

The rootfs for SCP-P4080-2G-ENP2 include RAMDISK and NFS.

Commands

1. `make rootfs`: The output image is `/local/tmp/<username>/rootfs_ext2.img`.
2. Build Targets supported for rootfs
   - `rootfs`: builds rootfs
   - `rootfs-ext2`: builds rootfs for ram disk
   - `rootfs-nfs`: builds rootfs for nfs
   - `rootfs-clean`: clean the rootfs

Output

The build images are `rootfs_ext2.img` and `rootfs_nfs.tar.gz` in the current working directory.

7.21.4 Build Misc Firmware

Misc Firmware for SCP-P4080-2G-ENP2 includes FMAN uCode and RCW image:

- FMAN uCode is `misc/fman_ucode/fsl_fman_ucode_P3_P4_P5_101_8.bin`
- RCW image is `misc/rcw/rcw.bin`

7.22 Deploy BSP Images

This section explains how to deploy BSP images. Assuming that you have built a BSP release package `COMX_P4080_V100B00.tar.gz` by running `./build.sh V100B00` located at `/local/ tmp/`.

7.22.1 Pre-Deployment Steps

The following steps must be performed before deployment:

1. Connect the board to your network using a network cable to the RGMII Ethernet port.
2. Setup a TFTP server in this network. Assuming that the IP address of this server is 192.168.0.100 and the root directory is `/tftpboot/`.
3. Create a `comx_p4080/ in /tftpboot/` subdirectory.
4. Copy the `COMX_P4080_<Version_Number>.tar.gz` file into the directory `/tftpboot/`

   `comx_p4080/` on TFTP server.
5. Change current directory to `/tftpboot/comx_p4080/`.
6. Extract the `.tar.gz` file to the current directory. The following files are extracted to the `COMX_P4080_V100B00/`:
   - `comx.dtb`
   - `rcw.bin`
   - `rcw-codewarrior.bin`
   - `rootfs_ext2.img`
   - `rootfs_nfs.tar.gz`

- `uImage`
- `fsl_fman_ucode_P3_P4_P5_101_8.bin`
- `u-boot.bin`

7. Extract the `rootfs_nfs.tar.gz` file to the `/tftpboot/comx_p4080/` location using the `sudo tar xzvf COMX_P4080_V100B00/rootfs_nfs.tar.gz`.
8. Add `/tftpboot/comx_p4080/rootfs_nfs/` to NFS exports list in `/etc/exports`:
   `/tftpboot/comx_p4080/rootfs_nfs *(rw,sync,no_root_squash)`
9. Restart NFS service to export `/tftpboot/comx_p4080/rootfs_nfs/` using the `sudo/sbin/service nfs` restart command.
10. The following commands should be executed in U-Boot command line:
    - Setup the U-Boot environment variables for the network settings. Example:
      ```
      => setenv ethaddr 00:01:af:12:23:01
      => setenv ipaddr 192.168.0.99
      => setenv netmask 255.255.255.0
      => setenv gatewayip 192.168.0.1
      => setenv serverip 192.168.0.100
      => setenv ethact FM1@DTSEC1
      ```
    - Setup the U-Boot environment variables for upgrade files. Example:
      ```
      => setenv rcwfile comx_p4080/COMX_P4080_V100B00/rcw.bin
      => setenv fmanfile
      comx_p4080/COMX_P4080_V100B00/fsl_fman_ucode_P3_P4_P5_101_8.
      bin
      => setenv bootfile comx_p4080/COMX_P4080_V100B00/uImage
      => setenv norfsfile
      comx_p4080/COMX_P4080_V100B00/rootfs_ext2.img
      => setenv fdtfile comx_p4080/COMX_P4080_V100B00/comx.dtb
      => setenv ubootfile comx_p4080/COMX_P4080_V100B00/u-boot.bin
      => setenv rootpath /tftpboot/comx_p4080/rootfs_nfs
      ```

- Test that the network and filename settings can download the files successfully. Example:

```
=> tftpboot $loadaddr $rcwfile
=> tftpboot $loadaddr $fmanfile
=> tftpboot $loadaddr $bootfile
=> tftpboot $loadaddr $norfsfile
=> tftpboot $loadaddr $fdtfile
=> tftpboot $loadaddr $ubootfile
```

7.22.2 Deploying BSP Images on NOR FLASH

Following are the steps to deploy BSP images on NOR FLASH:

1. Upgrade RCW, FMAN uCode, kernel, RAMDISK image, U-Boot and DTB on NOR FLASH individually. Example:

```
=> run updrcw; run updfman; run updkernel; run updnorfs; run
updfdt; run updubootboot
```

2. Erase previous U-Boot environment settings using the => `run eraenv` command.
3. Reset the board using the => `reset` command. The board will boot up with new BSP.

7.23 Boot

COMX-P40x0 ENP2 provides the following boot methods:

- *RAMboot*
- *NORboot*
- *NANDboot*
- *NFSboot*
- *USBFATboot and USBEXT2boot*
- *MMCFATboot and MMCEXT2boot*

Common device environment variables in U-Boot include the following:

- uart# and consoledev

  0 - ttyS0

  1 - ttyS1

  2 - ttyS2

  3 - ttyS3

- ethact and netdev

7.23.1 RAMboot

The COMX-P40x0 ENP2 has a U-Boot variable called "ramboot".

```
setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate
$hwbootargs $othbootargs;tftp $ramdiskaddr $ramdiskfile;tftp
$loadaddr $bootfile;tftp $fdtaddr $fdtfile;bootm $loadaddr
$ramdiskaddr $fdtaddr
```

"ramboot" will first load RAMDISK, Linux kernel and DTB into RAM through network by TFTP then boot.

The following are the critical environment variables for "ramboot":

ethact	-	Active ethernet port
ramdiskfile	-	RAMDISK file name on TFTP server
bootfile	-	Linux kernel file name on TFTP server
fdtfile	-	DTB file name on TFTP server

The following are the examples of critical environment variables:

=> setenv ethact FM1@DTSEC1

=> setenv ramdiskfile comx_p4080/COMX_P4080_V100R00/rootfs_ext2.img

=> setenv bootfile comx_p4080/COMX_P4080_V100R00/uImage

=> setenv fdtfile comx_p4080/COMX_P4080_V100R00/comx.dtb

7.23.2 NORboot

The COMX-P40x0 ENP2 has a U-Boot variable called "norboot"

```
setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate
$hwbootargs $othbootargs;bootm $norbootaddr $norfsaddr $norfdtaddr
```

"norboot" will load RAMDISK, Linux kernel and DTB from NOR Flash into RAM then boot.

The following are the critical environment variables for "norboot":

norfsaddr	-	RAMDISK address on NOR FLASH
norbootaddr	-	Linux kernel address on NOR FLASH
norfdtaddr	-	DTB address on NOR FLASH

The following are the examples of critical environment variables:

=> setenv norfsaddr E9000000

=> setenv norbootaddr EE000000

=> setenv norfdtaddr EFD00000

7.23.3 NANDboot

The COMX-P40x0 ENP2 has a U-Boot variable called "nandboot".

```
nandboot=setenv bootargs root=/dev/$jffs2nand rw
console=$consoledev,$baudrate rootfstype=jffs2 $hwbootargs
$othbootargs;bootm $norbootaddr - $norfdtaddr
```

The "nandboot" will load Linux kernel and DTB from NOR flash into RAM and then boot. JFFS2 will then mount on the file system on NAND flash as rootfs.

The following are the critical environment variables for "nandboot":

jffs2nand	-	MTD device for JFFS2 rootfs on NAND FLASH
norbootaddr	-	Linux kernel address on NOR FLASH
norfdtaddr	-	DTB address on NOR FLASH

The following are the examples of critical environment variables:

=> setenv jffs2nand mtdblock7

=> setenv norbootaddr EE000000

=> setenv norfdtaddr EFD00000

7.23.4 NFSboot

The COMX-P40x0 ENP2 has a U-Boot variable called "nfsboot".

```
setenv bootargs root=/dev/nfs rw nfsroot=$serverip:$rootpath
ip=$ipaddr:$serverip:$gatewayip:$netmask:$hostname:$netdev:off
console=$consoledev,$baudrate $hwbootargs $othbootargs;tftp
$loadaddr $bootfile;tftp $fdtaddr $fdtfile;bootm $loadaddr -
$fdtaddr
```

The "nfsboot" will load Linux kernel and DTB into RAM via network by TFTP and then boot. NFS will then mount on the remote server as rootfs.

The following are the critical environment variables for "nfsboot":

ethact	-	Active ethernet port
netdev	-	The NFS mounting network port
bootfile	-	Linux kernel file name on TFTP server
fdtfile		DTB file name on TFTP server
rootpath		The NFS path the remote server exports

The following are the examples of critical environment variables:

=> setenv ethact FM1@DTSEC1

=> setenv netdev eth0

=> setenv bootfile comx_p4080/COMX_P4080_V100R00/uImage

=> setenv fdtfile comx_p4080/COMX_P4080_V100R00/comx.dtb

=> setenv rootpath /tftpboot/comx_p4080/rootfs_nfs

7.23.5 USBFATboot and USBEXT2boot

The COMX-P40x0 ENP2 has a U-Boot variable called "usbfatboot".

```
setenv bootargs root=/dev/$usbbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs $othbootargs;usb
start;fatload usb 0:1 $loadaddr /boot/$bootfile;fatload usb 0:1
$fdtaddr  /boot/$fdtfile;bootm $loadaddr - $fdtaddr
```

The COMX-P40x0 ENP2 has a U-Boot variable called "usbext2boot".

```
setenv bootargs root=/dev/$usbbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs $othbootargs;usb
start;ext2load usb 0:2 $loadaddr /boot/$bootfile;ext2load usb 0:2
$fdtaddr  /boot/$fdtfile;bootm $loadaddr - $fdtaddr
```

The "usbfatboot" will load Linux kernel and DTB from the FAT partition (1st partition) on USB stick into RAM and then boot. EXT2 partition (2nd partition) will be mounted on the USB stick as rootfs.

The "usbext2boot" will load Linux kernel and DTB from the EXT2 partition (2nd partition) on USB stick into RAM and then boot. Mounting it on the same partition on this USB stick will boot as rootfs

The following are the critical environment variables for "usbfatboot" and "usbext2bot":

bootfile	-	Linux kernel file name
fdtfile	-	DTB file name

The following are the examples of critical environment variables:

=> setenv bootfile COMX_P4080_V100R00/uImage

=> setenv fdtfile COMX_P4080_V100R00/comx.dtb

Users need to create two partitions on the USB stick. FAT32 is the first partition and the EXT2 is the second partition. Both partitions contain a directory /boot/ and the directory has kernel DTB files. EXT2 partition contains the rootfs which can be from rootfs_nfs.tar.gz

7.23.6 MMCFATboot and MMCEXT2boot

The COMX-P40x0 ENP2 has a U-Boot variable called "mmcfatboot".

```
setenv bootargs root=/dev/$mmcbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs
$othbootargs;mmcinfo;fatload mmc 0:1 $loadaddr
/boot/$bootfile;fatload mmc 0:1 $fdtaddr  /boot/$fdtfile;bootm
$loadaddr - $fdtaddr
```

The COMX-P40x0 ENP2 also has a U-Boot variable called "mmcext2boot".

```
setenv bootargs root=/dev/$mmcbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs
$othbootargs;mmcinfo;ext2load mmc 0:2 $loadaddr
/boot/$bootfile;ext2load mmc 0:2 $fdtaddr  /boot/$fdtfile;bootm
$loadaddr - $fdtaddr
```

The "mmcfatboot" will load Linux kernel and DTB from the FAT partition (1st partition) on MMC/SDHC card into RAM and then boot. EXT2 partition (2nd partition) will mount on this card as rootfs.

"mmcext2boot" will load Linux kernel and DTB from the EXT2 partition (2nd partition) on MMC/SDHC card into RAM and then boot. The same partition will mount on this card as rootfs.

The following are the critical environment variables for "mmcfatboot" and "mmcext2boot":

bootfile	-	Linux kernel file name
fdtfile	-	DTB file name

The following are the examples of critical environment variables:

```
=> setenv bootfile COMX_P4080_V100R00/uImage
=> setenv fdtfile COMX_P4080_V100R00/comx.dtb
```

Similar to the USB drive, users need to create two partitions on the MMC/SDHC card. FAT32 is the first partition and the EXT2 is the second partition. Both partitions contain a directory /boot/ and the directory has kernel DTB files. EXT2 partition contains the rootfs which can be from `rootfs_nfs.tar.gz`.

Related Documentation

A.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing/support/product/technical-documentation.php.
2. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
3. In the **Search** text box, type the product name and click GO.

Table A-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
COMX-P40x0 ENP2 Safety Notes Summary	6806800R99

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